19-3694; Rev 0; 10/05

MAXIM

SPI-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

General Description

The MAX6916 provides all the features of a real-time clock (RTC) plus a microprocessor supervisory circuit, NV RAM controller, and backup-battery monitor function. In addition, 96 x 8 bits of static RAM are available for scratchpad storage. The MAX6916 communicates with a microprocessor through an SPI™-bus-compatible serial interface.

The real-time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap years through 2099. The clock operates in either 24hr or 12hr format with an AM/PM indicator. A time/date-programmable alarm function is provided with an open-drain, active-low alarm output.

The microprocessor supervisory circuit features an open-drain, active-low reset available in three different reset thresholds. A manual reset input and a watchdog function are included as well.

The NV RAM controller provides power for external SRAM from a backup battery plus chip-enable gating. The backup battery also provides data retention of the on-board 96 x 8 bits of RAM. An open-drain, active-low, battery-on signal alerts the system when operating from a battery.

The battery-test circuitry periodically tests the backup battery for a low-battery condition. An optional external resistor network selects different battery thresholds. A freshness seal prevents battery drain until the first V_{CC} power-up.

The MAX6916 has a crystal-fail-detect circuit and a data-valid bit. The MAX6916 is available in a 20-pin QSOP package and is guaranteed to operate over the -40°C to +85°C extended temperature range.

Applications

Point-of-Sale Equipment

Programmable Logic Controllers

Intelligent Instruments

Fax Machines

Digital Thermostats

Industrial Controls

Pin Configuration and Selector Guide appear at end of data sheet.

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Features

- **Real-Time Clock Counts**
  Seconds, Minutes, Hours, Date, Month, Day of Week, and Year with Leap-Year Compensation Through 2099
- **4MHz SPI-Bus-Compatible Interface at 5V, 2MHz at 3V, and 3.3V**
- **SPI Interface Supports Modes 1 and 3 (0, 1 and 1, 1)**
- **96 x 8 Bits of RAM for Scratchpad Data Storage**
- **Uses Standard 32.768kHz, 6pF Load, Watch Crystal**
- **Single-Byte or Multiple-Byte (Burst Mode) Data Transfer for Read or Write of Clock Registers or RAM**
- **Battery Monitor and Low-Battery Warning Output**
  Internal Default for Lithium Backup-Battery Testing
  Pins Available for Other Backup-Battery Testing Configurations
- **Dual Power-Supply Pins for Primary and Backup Power**
- **Battery-On Output**
- **NV RAM Controller**
  Chip-Enable Gating (Control of $\overline{CE}$ with Reset and Power Valid)
  V_{OUT} for SRAM Power
- **µP Supervisor with Watchdog Input**
- **Programmable Time/Date Alarm Output**
- **Data Valid Bit (Loss of All Voltage Alerts User of Corrupt Data)**
- **Crystal-Fail Detect**
- **Small 20-Pin, QSOP Surface-Mount Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX6916EO30+	-40°C to +85°C	20 QSOP	E20-2
MAX6916EO33+	-40°C to +85°C	20 QSOP	E20-2
MAX6916EO50+	-40°C to +85°C	20 QSOP	E20-2

+Denotes lead-free package.

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ABSOLUTE MAXIMUM RATINGS

V_{BATT}, V_{CC} to GND .....-0.3V to +6.0V
All Other Pins to GND.....-0.3V to (V_{CC} + 0.3V)
All Other Pins to GND.....-0.3V to (V_{BATT} + 0.3V)
Input Currents
V_{CC} 200mA
V_{BATT} 20mA
GND 20mA
All Other Pins.....±20mA
Output Currents
V_{OUT} Continuous 200mA
All Other Outputs 20mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin QSOP (derate 9.1mW/°C over +70°C).....727mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range (Note 3)	V_{CC}	MAX6916EO30		2.7	3.0	3.3	V
		MAX6916EO33		3.0	3.3	3.6	
		MAX6916EO50		4.5	5.0	5.5	
Operating Voltage Range BATT (Note 4)	V_{BATT}	MAX6916EO30		2.0		5.5	V
		MAX6916EO33		2.0		5.5	
		MAX6916EO50		2.0		5.5	
Timekeeping Current V_{BATT} (Note 5)	I_{BATT}	XTAL FAIL disabled	V_{BATT} = 2V, V_{CC} = 0			1	µA
			V_{BATT} = 3V, V_{CC} = 0			1.4	
			V_{BATT} = 3.6V, V_{CC} = 0			1.9	
			V_{BATT} = 5.5V, V_{CC} = 0			3.8	
		XTAL FAIL enabled	V_{BATT} = 2V, V_{CC} = 0			1.23	
			V_{BATT} = 3V, V_{CC} = 0			1.61	
			V_{BATT} = 3.6V, V_{CC} = 0			2.3	
			V_{BATT} = 5.5V, V_{CC} = 0			4.08	
Active Supply Current V_{CC} (Note 6)	I_{CCA}	XTAL FAIL disabled	V_{CC} = 3.3V, V_{BATT} = 0			0.35	mA
			V_{CC} = 3.6V, V_{BATT} = 0			0.4	
			V_{CC} = 5.5V, V_{BATT} = 0			1.1	
		XTAL FAIL enabled	V_{CC} = 3.3V, V_{BATT} = 0			0.36	
			V_{CC} = 3.6V, V_{BATT} = 0			0.42	
			V_{CC} = 5.5V, V_{BATT} = 0			1.2	
Standby Current V_{CC} (Note 5)	I_{CCS}	XTAL FAIL disabled	V_{CC} = 3.3V, V_{BATT} = 0			20	µA
			V_{CC} = 3.6V, V_{BATT} = 0			25	
			V_{CC} = 5.5V, V_{BATT} = 0			76	
		XTAL FAIL enabled	V_{CC} = 3.3V, V_{BATT} = 0			27	
			V_{CC} = 3.6V, V_{BATT} = 0			30	
			V_{CC} = 5.5V, V_{BATT} = 0			81	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OUT}						
V_{OUT} in V_{CC} Mode (Note 4)	V_{OUT}	V_{CC} = 2.7V, V_{BATT} = 0, I_{OUT} = 35mA	V_{CC} - 0.2			V
		V_{CC} = 3.0V, V_{BATT} = 0, I_{OUT} = 35mA	V_{CC} - 0.2			
		V_{CC} = 4.5V, V_{BATT} = 0, I_{OUT} = 70mA	V_{CC} - 0.2			
V_{OUT} in Battery-Backup Mode (Notes 4, 7)	V_{OUT}	V_{BATT} = 2V, V_{CC} = 0, I_{OUT} = 400µA	V_{BATT} - 0.02			V
		V_{BATT} = 3V, V_{CC} = 0, I_{OUT} = 800µA	V_{BATT} - 0.03			
		V_{BATT} = 4.5V, V_{CC} = 0, I_{OUT} = 1.5mA	V_{BATT} - 0.05			
V_{BATT}-to-V_{CC} Switchover Threshold	V_{TRU}	Power-up (V_{CC} < V_{RST}) switch from V_{BATT} to V_{CC} (Note 7)		V_{BATT} + 0.1		V
V_{CC}-to-V_{BATT} Switchover Threshold	V_{TRD}	Power-down (V_{CC} < V_{RST}) switch from V_{CC} to V_{BATT} (Note 7)		V_{BATT} - 0.1		V
$\overline{CE\_IN}$ AND $\overline{CE\_OUT}$ (Figures 7, 11, 12, 13)						
$\overline{CE\_IN}$ Leakage Current	I_{IL}, I_{IH}	Disabled, V_{CC} < V_{RST}, $V_{\overline{CE\_IN}}$ = V_{CC} or GND	-1		+1	µA
$\overline{CE\_IN}$-to-$\overline{CE\_OUT}$ Resistance		V_{CC} = $V_{CC(MIN)}$, V_{IH} = 0.9V_{CC}, $\overline{CE\_OUT}$ = GND, V_{IL} = 0.1V_{CC}, $\overline{CE\_OUT}$ = V_{CC}		46	140	Ω
$\overline{CE\_IN}$-to-$\overline{CE\_OUT}$ Propagation Delay	t_{CED}	50Ω source impedance driver, C_{LOAD} = 10pF, V_{CC} = $V_{CC(MIN)}$, V_{IH} = 0.9V_{CC}, V_{IL} = 0.1V_{CC} (Note 8); measured from 50% point on $\overline{CE\_IN}$ to the 50% point of $\overline{CE\_OUT}$		10	20	ns
$\overline{RESET}$ Active to $\overline{CE\_OUT}$ High Delay	t_{RCE}	$\overline{MR}$ high to low	2	10	50	µs
$\overline{CE\_OUT}$ Active-Low Delay after V_{CC} > V_{RST}	t_{RP}		140	200	280	ms
$\overline{CE\_OUT}$ Output High Voltage	V_{OH}	I_{OH} = -100µA, V_{BATT} = 2V, V_{CC} = 0, $\overline{RESET}$ = low	0.8 x V_{BATT}			V
$\overline{MR}$ INPUT (Figure 7)						
$\overline{MR}$ Input Voltage	V_{IL}				0.8	V
	V_{IH}		2.0			
$\overline{MR}$ Pullup Resistance		Internal pullup resistor		50		kΩ
$\overline{MR}$ Minimum Pulse Width			1			µs
$\overline{MR}$ Glitch Immunity	t_{GW}				35	ns
$\overline{MR}$ to $\overline{RESET}$ Delay	t_{RD}	V_{CC} = $V_{CC(MIN)}$, V_{BATT} = 0		450	600	ns

SPI-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
WDI INPUT (Figure 9)							
WDI Initial Timeout Period		V_{CC} > V_{RST} from rising edge of $\overline{RESET}$		1.00	1.6	2.25	s
Watchdog Timeout Period	t_{WDL}	Long watchdog timeout period		1.00	1.6	2.25	s
	t_{WDS}	Short watchdog timeout period		140	200	280	ms
Minimum WDI Input Pulse Width	t_{WDI}			100			ns
WDI Input Threshold	V_{IL}					0.8	V
	V_{IH}			2.0			
WDI Input Leakage Current		V_{WDI} = V_{CC} or GND		-100		+100	nA
V_{CC} Standby Current with WDI Max Frequency	I_{CCSW}	Watchdog frequency = 1MHz, V_{CC} = $V_{CC(MAX)}$ (Note 5)				450	µA
BATTERY TEST AND TRIP (Figures 14, 15, and 16)							
V_{BATT} Trip Point	V_{BTP}	Internal mode		2.45	2.6	2.7	V
TRIP Input Threshold	V_{TRIP}	V_{CC} = $V_{CC(MAX)}$, V_{BATT} = 2V, external mode		1.14	1.24	1.31	V
TRIP Input Comparator Hysteresis	V_{TRIP_HYST}				10		mV
TRIP Input Current	I_{TRIP_LKG}	External mode		-100		+100	nA
Battery Test Load	R_{LOAD_INT}	Internal		0.5	0.91	1.3	MΩ
TEST Output High Voltage	V_{TEST_HIGH}	I_{TEST} = -5mA		V_{OUT} - 0.3V			V
TEST Output Low Voltage	V_{TEST_LOW}	I_{TEST} = 5mA				0.3	V
$\overline{BATT\_LO}$, $\overline{ALM}$ OUTPUT							
Output Low Voltage	V_{OL}	V_{BATT} = 2V, V_{CC} = 0, I_{OL} = 5mA				0.5	V
	V_{OL}	V_{CC} = 2.7V, V_{BATT} = 0, I_{OL} = 10mA				0.5	
	V_{OL}	V_{CC} = 4.5V, V_{BATT} = 0, I_{OL} = 20mA				0.5	
Off-Leakage	I_{LKG}			-100		+100	nA
$\overline{BATT\_ON}$ OUTPUT							
Output Low Voltage	V_{OL}	V_{BATT} = 2V, V_{CC} = 0, I_{OL} = 5mA				0.5	V
	V_{OL}	V_{BATT} = 2.7V, V_{CC} = 0, I_{OL} = 10mA				0.5	
	V_{OL}	V_{BATT} = 4.5V, V_{CC} = 0, I_{OL} = 20mA				0.5	
Off-Leakage	I_{LKG}			-100		+100	nA
$\overline{RESET}$							
$\overline{RESET}$ Threshold Voltage	V_{RST}	MAX6916EO30		2.5	2.63	2.7	V
		MAX6916EO33		2.8	2.93	3.0	
		MAX6916EO50		4.1	4.38	4.5	
V_{RST} Hysteresis	V_{HYST}				30		mV
V_{CC} Falling-Reset Delay	t_{RPD}	V_{CC} falling from $V_{RST(MAX)}$ to $V_{RST(MIN)}$ measured from the beginning of V_{CC} falling to $\overline{RESET}$ low	MAX6916EO30		27	75	µs
			MAX6916EO33		37	90	
			MAX6916EO50		50	120	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Reset Active-Timeout Period	t_{RP}		140	200	280	ms
$\overline{RESET}$ Output-Low Voltage	V_{OL}	$\overline{RESET}$ asserted, I_{OL} = 1.6mA, V_{BATT} = 2V, V_{CC} = 0			0.2	V
Off-Leakage	I_{LKG}		-100		+100	nA
SPI DIGITAL INPUTS DIN, SCLK, $\overline{CS}$						
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{HYS}			0.05 x V_{CC}		V
Input Leakage Current		V_{IN} = 0 to V_{CC}	-100		+100	nA
Input Capacitance		(Note 8)			10	pF
SPI DIGITAL OUTPUT DOUT						
Output High Voltage	V_{OH}	I_{OH} = -1.6mA	0.9 x V_{CC}			V
Output Low Voltage	V_{OL}	I_{OL} = 1.6mA			0.4	V
Output Capacitance		(Note 8)			10	pF
Output Off-State Leakage Current	I_{OZ}		-100		+100	nA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI BUS TIMING (Figure 2 (Note 9))						
Maximum-Input Rise Time	t_{RIN}	DIN, SCLK, $\overline{CS}$		2		µs
Maximum-Input Fall Time	t_{FIN}	DIN, SCLK, $\overline{CS}$		2		µs
Output Rise Time	t_{ROUT}	DOUT, C_{LOAD} = 100pF		10		ns
Output Fall Time	t_{FOUT}	DOUT, C_{LOAD} = 100pF		10		ns
SLCK Period	t_{CP}	MAX6916EO30, MAX6916EO33	500			ns
		MAX6916EO50	238			
SCLK High Time	t_{CH}	MAX6916EO30, MAX6916EO33	200			ns
		MAX6916EO50	100			
SCLK Low Time	t_{CL}	MAX6916EO30, MAX6916EO33	200			ns
		MAX6916EO50	100			
SCLK Fall to DOUT Valid	t_{DO}	C_{LOAD} = 100pF			100	ns
DIN-to-SCLK Setup Time	t_{DS}		100			ns
DIN-to-SCLK Hold Time	t_{DH}		0			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
$\overline{CS}$ High Pulse Width	t_{CSW}		200			ns
$\overline{CS}$ High-to-DOUT High Impedance	t_{CSZ}				100	ns
$\overline{CS}$ to SCLK Setup Time	t_{CSS}		100			ns
BATTERY TEST TIMING (Figure 15)						
Battery Test to $\overline{BATT\_LO}$ Active	t_{BL}	(Note 8)			1	s

SPI-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Battery Test Cycle—Normal	t_{BTCN}	(Note 8)		24		hr
Battery Test Pulse Width	t_{BTPW}	(Note 8)			1	s

Note 1: V_{RST} is the reset threshold for V_{CC}. See the *Ordering Information*.

Note 2: All parameters are 100% tested at T_A = +85°C. Limits over temperature are guaranteed by design and are not production tested.

Note 3: The SPI serial interface is operational for $V_{CC} > V_{RST}$.

Note 4: See the *Detailed Description* (V_{OUT} function).

Note 5: I_{CCS} is specified with $\overline{CS}$ = V_{CC}, SCLK = DIN = WDI = $\overline{CE\_IN}$ = GND, DOUT, V_{OUT}, $\overline{CE\_OUT}$, and $\overline{MR}$ floating. I_{BATT} is specified with WDI = $\overline{CE\_IN}$ = SCLK = DIN = GND, $\overline{CS}$ = V_{CC}, DOUT, V_{OUT}, $\overline{CE\_OUT}$, and $\overline{MR}$ floating.

Note 6: I_{CCA} is specified with SCLK = 4MHz for V_{CC} = +5.5V and SCLK = 2MHz for V_{CC} = +3.3V and +3.6V. DOUT = OPEN, $\overline{CS}$ = GND, DIN = V_{CC}, $\overline{CE\_IN}$ = V_{CC}, V_{OUT} and $\overline{CE\_OUT}$ open, WDI = V_{CC} or GND.

Note 7: For OUT switchover to BATT, V_{CC} must fall below V_{RST} and V_{BATT}. For OUT switchover to V_{CC}, V_{CC} must be above V_{RST} or above V_{BATT}.

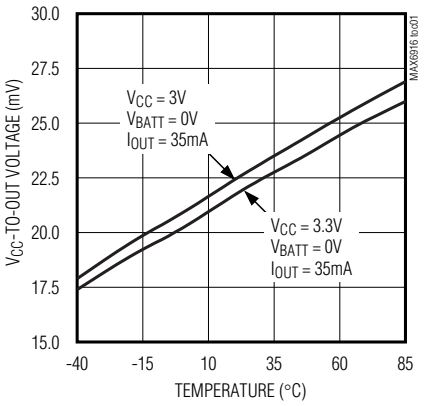
Note 8: Guaranteed by design. Not subject to production testing.

Note 9: All values are referred to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

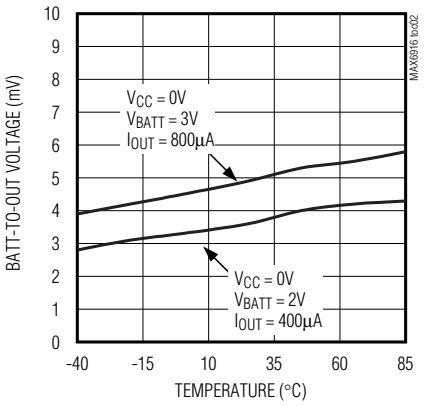
Typical Operating Characteristics

(V_{CC} = 3.3V, V_{BATT} = 3V, T_A = +25°C, unless otherwise noted.)

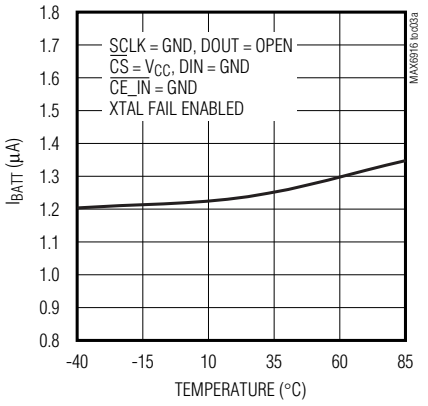
V_{CC}-TO-OUT VOLTAGE vs. TEMPERATURE



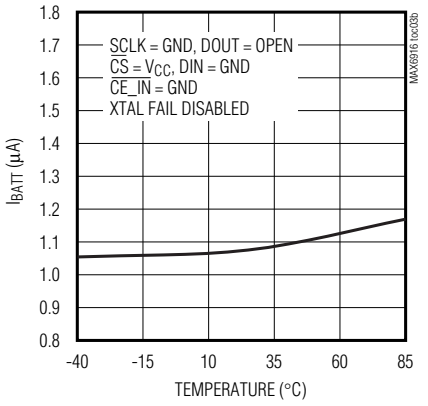
BATT-TO-OUT VOLTAGE vs. TEMPERATURE



TIMEKEEPING CURRENT vs. TEMPERATURE



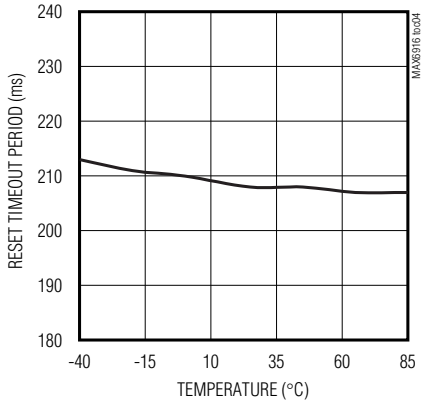
TIMEKEEPING CURRENT vs. TEMPERATURE



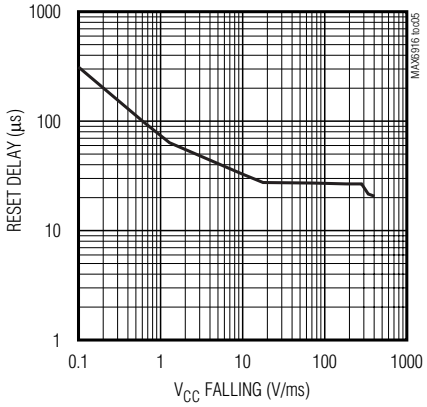
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, V_{BATT} = 3V, T_A = +25°C, unless otherwise noted.)

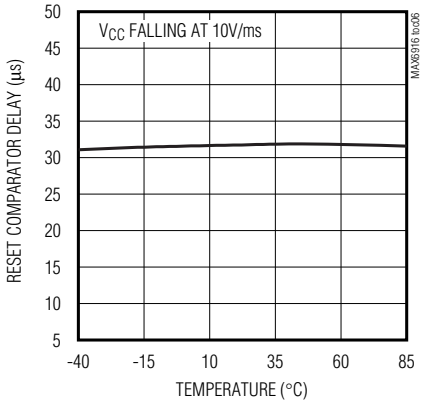
RESET TIMEOUT PERIOD vs. TEMPERATURE



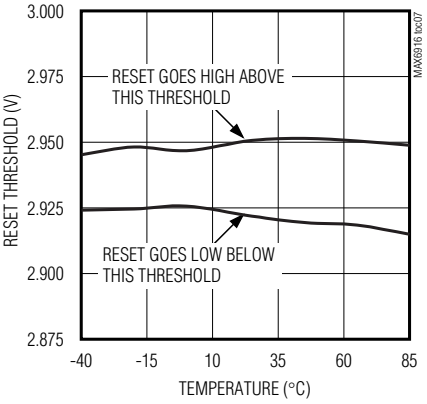
RESET COMPARATOR DELAY vs. V_{CC} FALLING



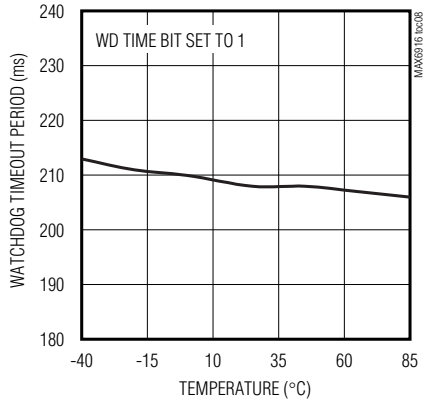
RESET COMPARATOR DELAY vs. TEMPERATURE



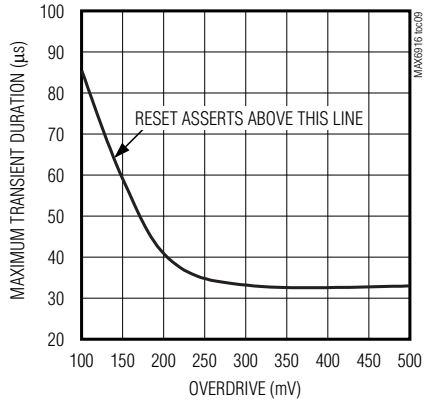
RESET THRESHOLD vs. TEMPERATURE (MAX6916E033)



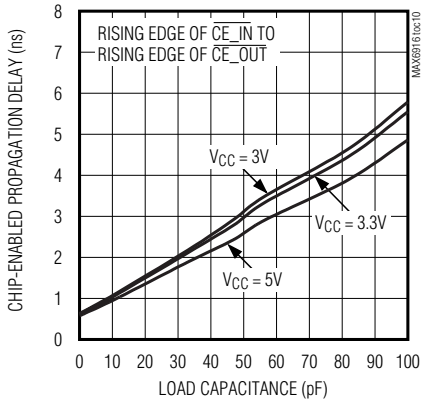
WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



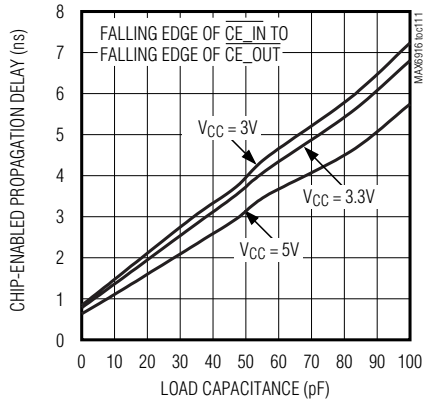
MAXIMUM TRANSIENT DURATION vs. RESET COMPARATOR OVERDRIVE



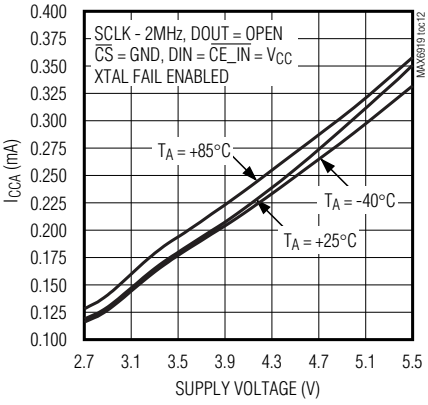
CHIP-ENABLED PROPAGATION DELAY vs. $\overline{CE\_OUT}$ LOAD CAPACITANCE (MAX6916E033)



CHIP-ENABLED PROPAGATION DELAY vs. $\overline{CE\_OUT}$ LOAD CAPACITANCE (MAX6916E033)



ACTIVE SUPPLY CURRENT vs. SUPPLY VOLTAGE

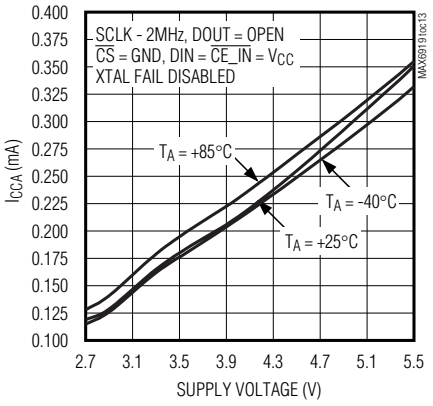


SPI-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

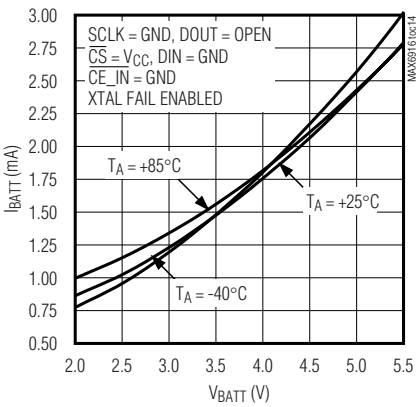
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, V_{BATT} = 3V, T_A = +25°C, unless otherwise noted.)

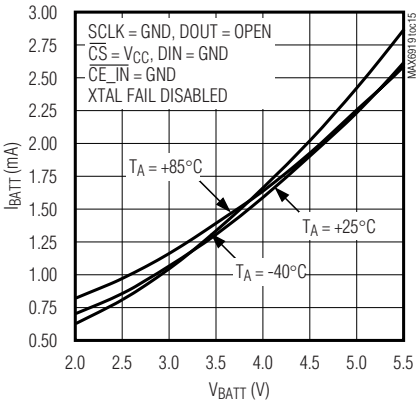
ACTIVE SUPPLY CURRENT vs. SUPPLY VOLTAGE



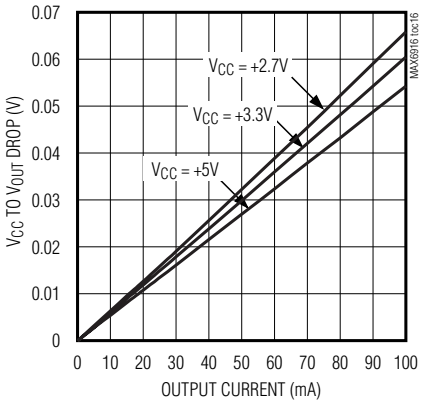
TIMEKEEPING CURRENT vs. SUPPLY VOLTAGE



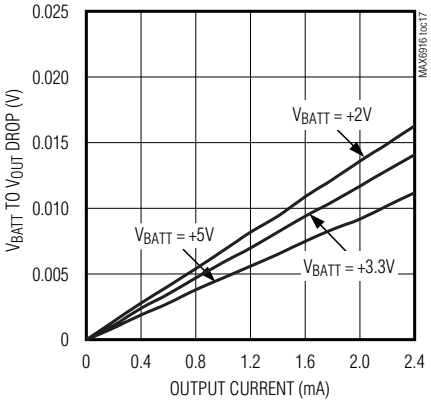
TIMEKEEPING CURRENT vs. SUPPLY VOLTAGE



VCC TO VOUT DROP vs. OUTPUT CURRENT (NORMAL MODE)



VBATT TO VOUT DROP vs. OUTPUT CURRENT (BATTERY BACKUP MODE)



Pin Description

PIN	NAME	FUNCTION
1	V_{OUT}	Supply Output for External SRAM or Other ICs Requiring Use of Backup Battery Power. When V_{CC} rises above the reset threshold or above V_{BATT}, V_{OUT} is connected to V_{CC}. When V_{CC} falls below V_{RESET} and V_{BATT}, V_{BATT} is connected to V_{OUT}. Connect a 0.1µF low-leakage bypass capacitor from V_{OUT} to GND. Leave open if not used.
2	TEST	External Battery Test. Active high for 1s during each battery test. Intended to drive an external MOSFET or bipolar transistor for an external battery-test configuration. External test must be selected in the control register to use TEST; otherwise, it remains low. Leave open if not used.
3	TRIP	External Trip Set. If a different battery-low threshold is desired other than the internal POR default of V_{BTP}, then connect R_{SET+} between V_{BATT} and TRIP and R_{SET-} between TRIP and the drain or collector of an external transistor whose base or gate is connected to TEST; see Figure 14 (see the *Battery Test* section). External test must be selected in the control register to use TRIP. Leave open if not used.
4	$\overline{BATT\_ON}$	Open-Drain, Battery-On Indicator. $\overline{BATT\_ON}$ is active low when the MAX6916 is powered from V_{BATT}.
5	$\overline{CE\_IN}$	Chip-Enable Input. The input to the chip-enable gating circuitry. Connect $\overline{CE\_IN}$ to GND if unused.
6	$\overline{MR}$	Manual-Reset Input. A logic-low on $\overline{MR}$ asserts $\overline{RESET}$. $\overline{RESET}$ remains asserted as long as $\overline{MR}$ is low and for t_{RP} after $\overline{MR}$ returns high. The active-low $\overline{MR}$ input has an internal pullup resistor. $\overline{MR}$ can be driven from a TTL- or CMOS-logic line or shorted to ground with a switch. Internal debouncing circuitry ensures noise immunity. Leave $\overline{MR}$ open if unused.
7	WDI	Watchdog Input. If WDI remains either high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and $\overline{RESET}$ is asserted. The internal watchdog timer clears while $\overline{RESET}$ is asserted or when WDI sees a rising or falling edge. The watchdog function can be disabled from the control register. The timeout period is configurable in the control register for 200ms or 1.6s.
8	GND	Ground
9	X1	32.768kHZ Crystal-Oscillator Input
10	X2	32.768kHZ Crystal-Oscillator Output

SPI-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

Pin Description (continued)

PIN	NAME	FUNCTION
11	DIN	SPI Serial Bus Data Input
12	$\overline{CS}$	SPI Serial Bus Chip-Select Input. Drive $\overline{CS}$ low to initiate a data transfer.
13	DOUT	SPI Serial Bus Data Output
14	SCLK	SPI Serial Bus Clock Input
15	$\overline{ALM}$	Open-Drain, Active-Low Alarm Output. $\overline{ALM}$ goes low when RTC time matches alarm thresholds set in the alarm threshold registers. $\overline{ALM}$ stays low until cleared by reading or writing to the alarm configuration register or to any of the alarm threshold registers.
16	$\overline{CE\_OUT}$	Chip-Enable Output. $\overline{CE\_OUT}$ goes low only when $\overline{CE\_IN}$ is low and $\overline{RESET}$ is not asserted. If $\overline{CE\_IN}$ is low when $\overline{RESET}$ is asserted, $\overline{CE\_OUT}$ remains low for t_{RCE} or until $\overline{CE\_IN}$ goes high, whichever occurs first. $\overline{CE\_OUT}$ is pulled to V_{OUT}.
17	$\overline{BATT\_LO}$	Open-Drain, Battery-Low Indicator. $\overline{BATT\_LO}$ is active low when the V_{BATT} input is tested below V_{BTP} if the internal trip is selected in the control register (POR default). If external trip is selected in the control register, then $\overline{BATT\_LO}$ is active low when TRIP is less than V_{TRIP}.
18	$\overline{RESET}$	Open-Drain, Active-Low Reset Output. $\overline{RESET}$ pulses low for t_{RP} when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is logic-low. $\overline{RESET}$ remains low for t_{RP} after either V_{CC} rises above the reset threshold or $\overline{MR}$ goes from low to high.
19	V_{CC}	Main Supply Input. Connect a 0.1µF bypass capacitor from V_{CC} to GND.
20	V_{BATT}	Backup-Battery Input. When V_{CC} falls below the reset threshold and V_{BATT}, V_{OUT} switches from V_{CC} to V_{BATT}. When V_{CC} rises above V_{BATT} or the reset threshold, V_{OUT} reconnects to V_{CC}. V_{BATT} may exceed V_{CC}. Connect V_{BATT} to GND if no backup-battery supply is used. Connect a 0.1µF low-leakage bypass capacitor from V_{BATT} to GND.

Detailed Description

Functional Description

The MAX6916 contains eight 8-bit timekeeping registers, seven 8-bit alarm threshold registers, one status register, one control register, one alarm-configuration register, and 96 x 8 bits of SRAM. In addition to single-byte reads and writes to registers and RAM, there is a burst timekeeping register read/write command, a burst RAM read/write command, and a battery-test command that allows software-commanded testing of the backup battery at any time. An SPI-bus-compatible interface allows serial communication with a microprocessor. When V_{CC} is less than the reset threshold, the serial interface is disabled to prevent erroneous data from being written to the MAX6916. A microprocessor supervisory section and an NVRAM controller are provided for ease of implementation with microprocessor-based systems. A crystal-fail-detect circuit and a data-valid bit can be used to guarantee RAM data integrity and valid timekeeping data. Time and calendar data are stored in a binary-coded decimal (BCD) format. Figure 1 shows the functional diagram of the MAX6916.

Real-Time Clock

The RTC provides seconds, minutes, hours, day, date, month, and year information. The end of the months is automatically adjusted for months with fewer than 31 days, including corrections for leap years through 2099.

Crystal Oscillator

The MAX6916 uses an external, standard 6pF load watch crystal. No other external components are required for this timekeeping oscillator. Power-up oscillator start time is dependent mainly upon applied V_{CC} and ambient temperature. The MAX6916, because of its low timekeeping current, exhibits a typical startup time of 1s to 2s.

SPI-Compatible Interface

Interface the MAX6916 to a microcontroller using a 4-wire, serial peripheral interface (SPI). The SPI is a synchronous bus for address and data transfer and is used when interfacing with Motorola and other microcontrollers with an SPI port. Four connections are required for the interface: DOUT (serial data out), DIN (serial data in), SCLK (serial clock), and $\overline{CS}$ (chip select). The MAX6916 acts as a slave device and the

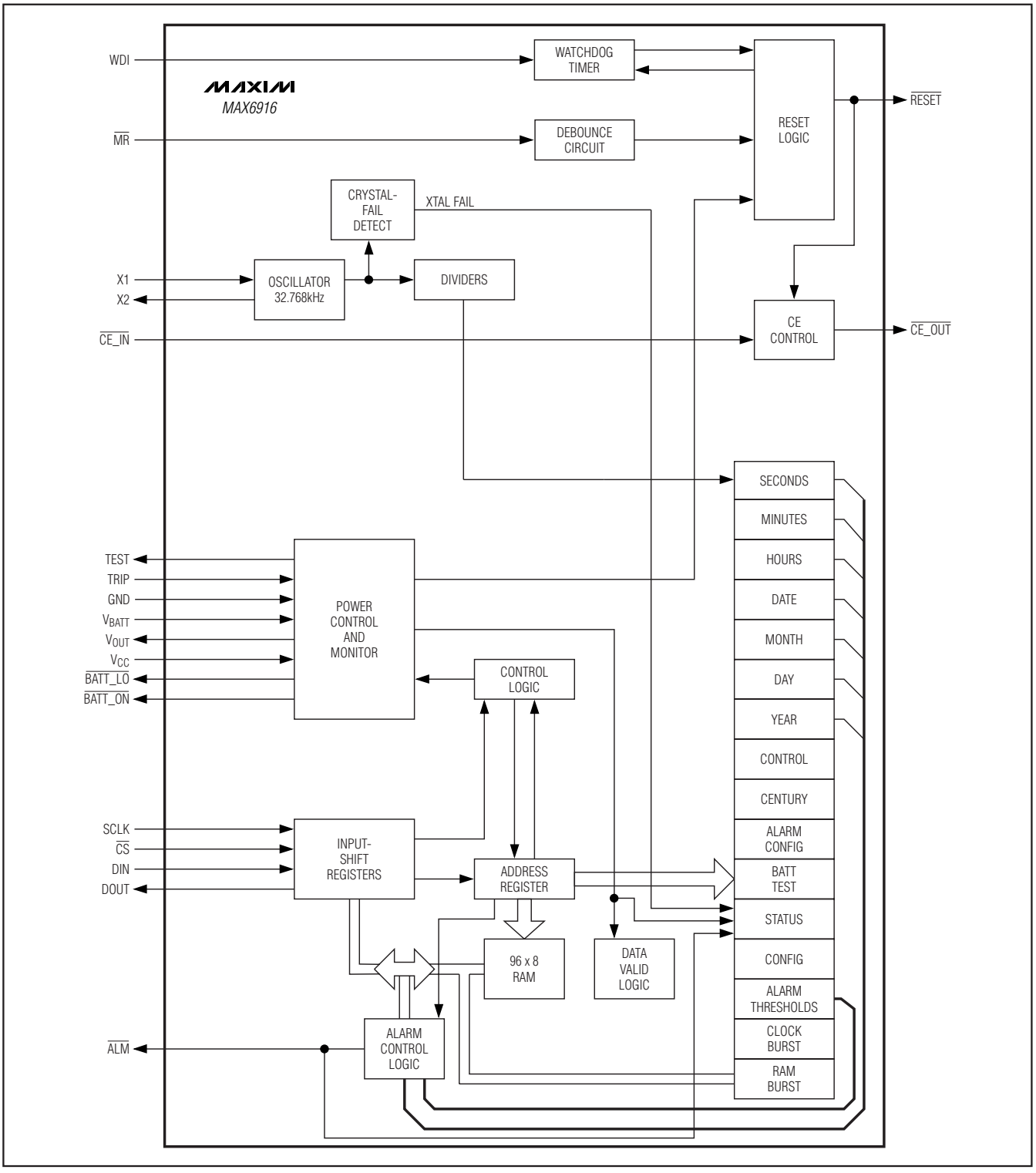


Figure 1. Functional Diagram

SPI-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

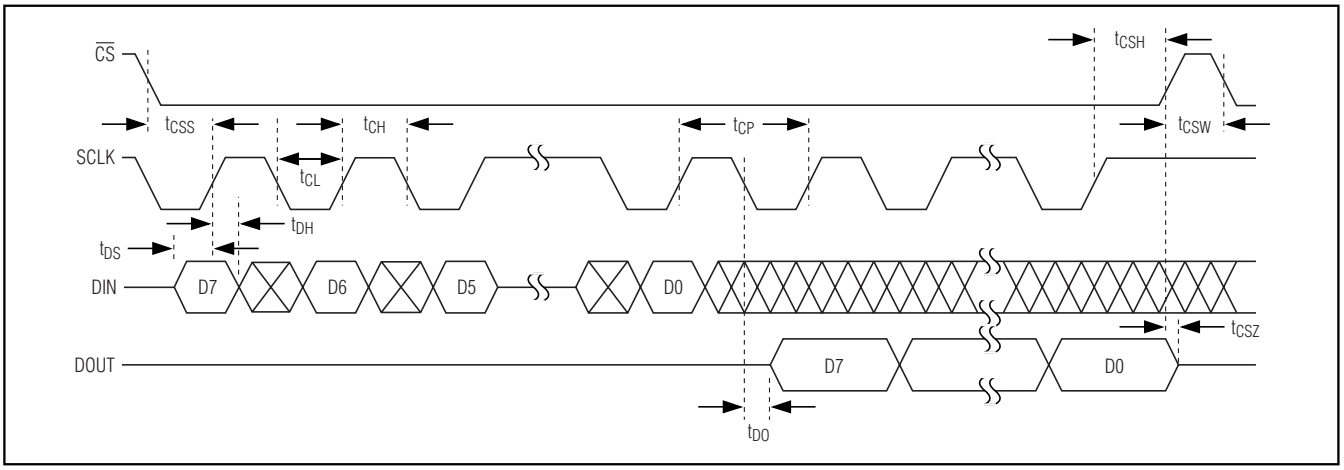


Figure 2. SPI Bus Timing Diagram

microcontroller acts as the master in an SPI application. $\overline{CS}$ is asserted low by the microcontroller to initiate a transfer and deasserted high to terminate a transfer. DIN transfers input data to the MAX6916 from the microcontroller, and DOUT transfers output data from the MAX6916 to the microcontroller. SCLK is used to synchronize data movement between the microcontroller and the MAX6916. SCLK, which is generated by the microcontroller, is active only during address and data transfer to any device on the SPI bus. The inactive clock polarity is usually programmable on the microcontroller side of the SPI interface. For the MAX6916, input data (DIN) is latched on the positive edge and output data (DOUT) is shifted out on the negative edge. There is one clock for each bit transferred. Address and data bits are transferred in groups of eight. Figure 2 shows an SPI bus timing diagram.

The SPI protocol allows for one of four combinations of serial clock phase and polarity from the microcontroller, through a 2-bit selection in its SPI control register. The clock polarity is specified by the CPOL control bit, which selects active-high or active-low clock, and has no significant effect on the transfer format. The clock-phase control bit, CPHA, selects one of two different transfer formats. The clock phase and polarity must be identical for the master and the slave. For the MAX6916, set the control bits to CPHA = 1 and CPOL = 1. This setting configures the system for data to be launched on the negative edge of SCLK and sampled on the positive edge. With CPHA equal to 1, $\overline{CS}$ can remain low between successive data byte transfers, allowing burst-mode data transfers to occur.

Address and data bytes are shifted, most significant bit (MSB) first, into the serial data input DIN of the MAX6916 and out of the serial data output DOUT. Data is shifted out at the negative edge of SCLK and shifted in or sampled at the positive edge of SCLK. Any transfer requires the address of the byte to be followed by 1 or more bytes of data. Data is transferred out of DOUT for a read operation and into DIN for a write operation. When not transferring data out, DOUT is put into a high-impedance state (Figure 2).

To maximize battery life and prevent erroneous data from being entered into the MAX6916, the serial bus interface is disabled when V_{CC} is below V_{RST} or when $\overline{RESET}$ is active.

In order to initiate SPI communications with the MAX6916, $\overline{CS}$ needs to be driven low, after which an address/command byte must be input. The address/command byte specifies the register to or from which information is to be transferred, as well as the nature of the transfer (read or write). After the address/command byte, 1 or more data bytes can be written or read. For a single-byte transfer, 1 byte is written or read and then $\overline{CS}$ is driven high by the microcontroller (Figures 3 and 5). For a multiple-byte transfer, however, multiple bytes can be read or written to the MAX6916 after the address/command byte has been written (Figures 4 and 6). In the case of burst operation, each read or write cycle causes the RTC register or RAM address to automatically increment. Incrementing continues (maximum value is 96 for RAM and 8 for register bank) until SPI transmission is terminated. To terminate the SPI transmission, drive $\overline{CS}$ high.

Address/Command Byte

Each data transfer into or out of the MAX6916 is initiated by an address/command byte. The address/command byte specifies which registers are to be accessed, and if the access is a read or write. The address command byte is input MSB (bit 7) first. Bit 7 determines if a read (logic 1) or write (logic 0) takes place. Data transfers can occur 1 byte at a time or in multiple-byte burst mode. Bits 6–0 specify the designated register or RAM location to be read or written to. Figures 3, 4, 5, and 6 show the different transfer operations that can take place with the MAX6916.

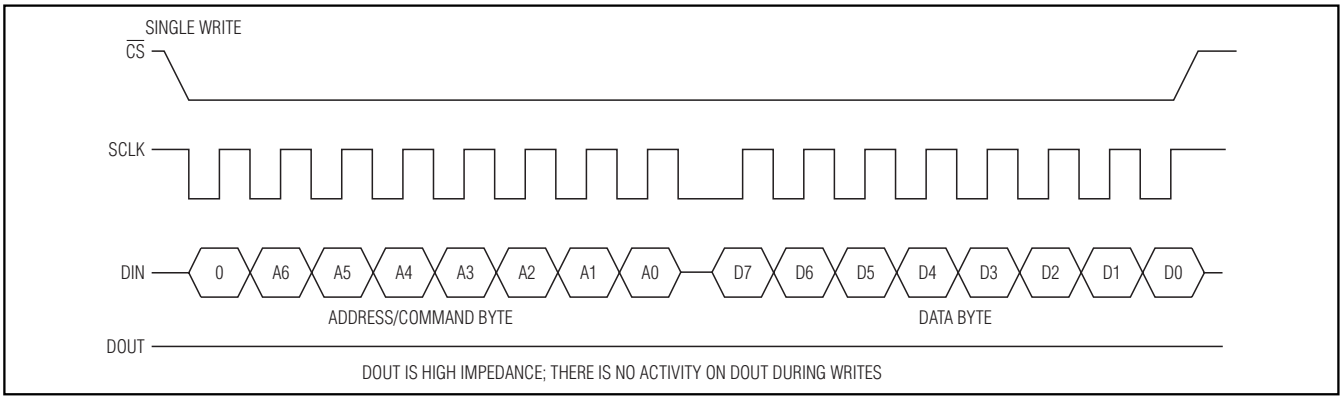


Figure 3. SPI Interface Single Write

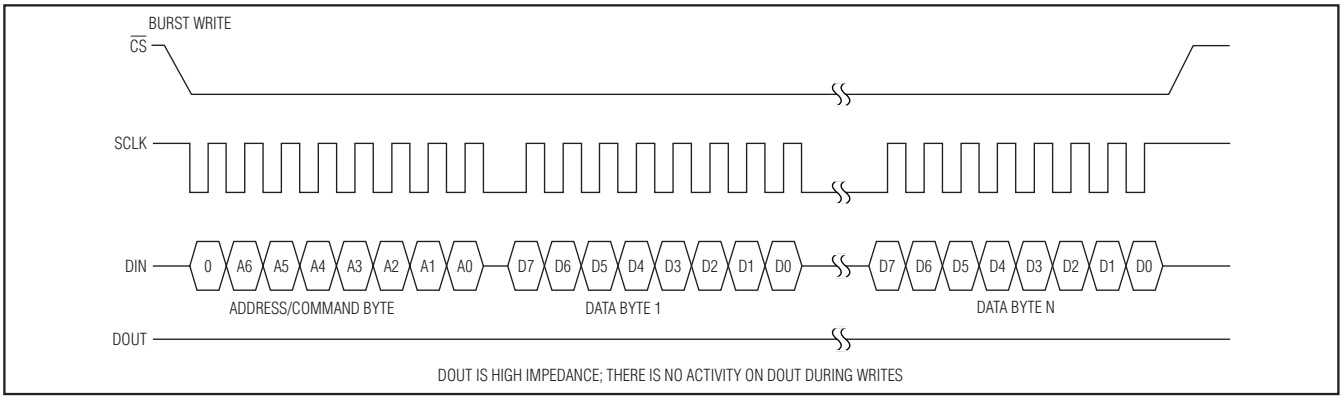


Figure 4. SPI Interface Multiple/Burst Write

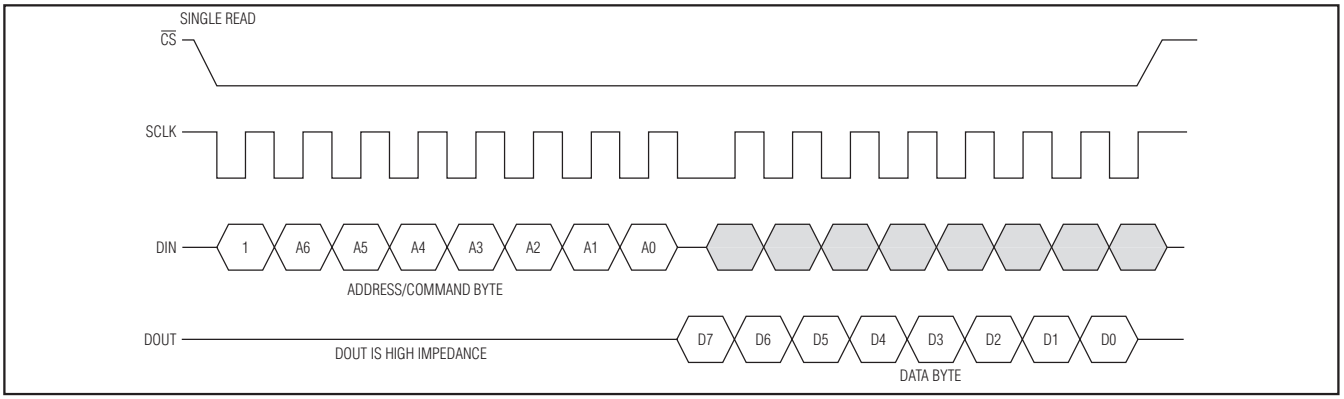


Figure 5. SPI Interface Single Read

SPI-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

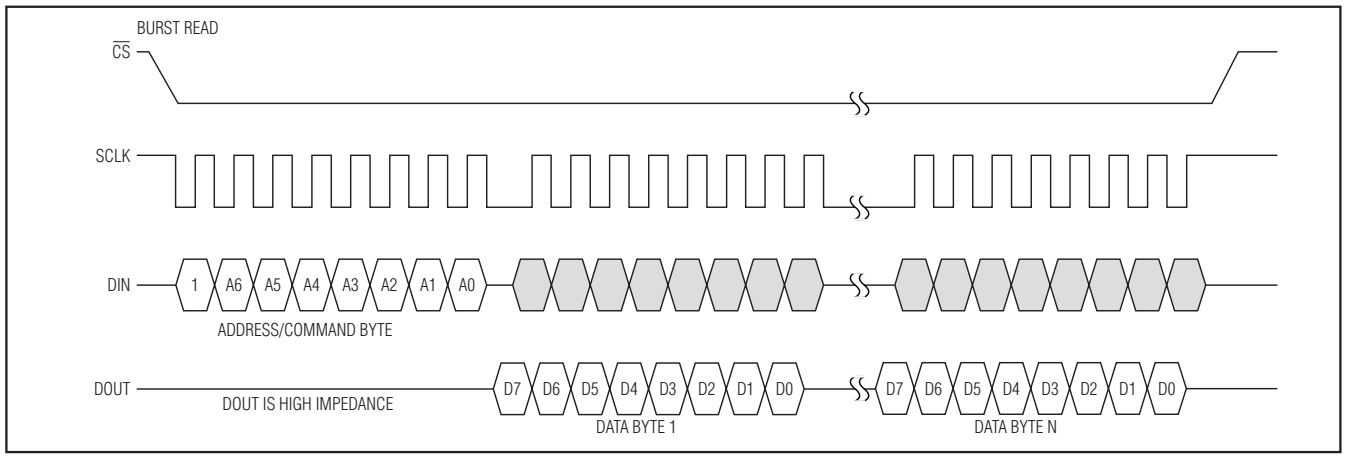


Figure 6. SPI Interface Multiple/Burst Read

Chip Select ($\overline{CS}$)

$\overline{CS}$ serves two functions. First, $\overline{CS}$ turns on the control logic that allows access to the shift register for address/command and data transfer. Second, $\overline{CS}$ provides a method of terminating either single-byte or multiple-byte data transfers. All data transfers are initiated by driving $\overline{CS}$ low. If $\overline{CS}$ is high, then DOUT is high impedance.

Serial Clock (SCLK)

A clock cycle on SCLK consists of a rising edge followed by a falling edge. For data input, data must be valid at DIN before the rising edge of the clock. For data outputs, bits are valid on DOUT after the falling edge of the clock.

Reading from the Timekeeping Registers

The timekeeping registers (seconds, minutes, hours, date, month, day, and year) and the control register can be read either with a single read (Figure 5) or a burst read (Figure 6). Since the RTC runs continuously and a read takes a finite amount of time, there is the possibility that the clock counters could change during a read operation, thereby reporting inaccurate timekeeping data. In the MAX6916, each clock counter's data is buffered by a latch. Clock counter data is latched by the SPI bus read command (on the falling edge of SCLK after the address/command byte has been sent by the master to read a timekeeping register). Collision-detection circuitry ensures that this does not happen coincident with a seconds counter update to ensure accurate time data is being read. This avoids time-data changes during a read operation. The clock counters continue to count and keep accurate time during the read operation.

If single reads are used to read each of the timekeeping registers individually, then it is necessary to do some error checking on the receiving end. An error can occur when the seconds counter increments before all the other registers are read out. For example, suppose a carry of 13:59:59 to 14:00:00 occurs during single-read operations of the timekeeping registers. Then the net data could become 14:59:59, which is erroneous real-time data. To prevent this with single-read operations, read the seconds register first (initial seconds) and store this value for future comparison. When the remaining timekeeping registers have been read out, read the seconds register again (final seconds). If the initial seconds value is 59, check that the final-seconds value is still 59; if not, repeat the entire single-read process for the timekeeping registers. A comparison of the initial-seconds value with the final-seconds value can indicate if there was a bus-delay problem in reading the timekeeping data (difference should always be 1s or less). Using a 2MHz bus speed, and sequential single reads, it would take under 75µs to read all seven of the timekeeping registers plus a second read of the seconds register.

The most accurate way to read the timekeeping registers is to perform a burst read. With burst reads, the main timekeeping registers (seconds, minutes, hours, date, month, day, year) and the control register are read sequentially, in the order listed with the seconds register first. They must be all read out as a group of eight registers, with 8 bytes each, for proper execution of the burst-read function. All seven timekeeping registers are latched upon the receipt of the burst-read command. Worst-case error that can occur between the actual time and the read time is 1s.

Writing to the Timekeeping Registers

The time and date can be set by writing to the timekeeping registers (seconds, minutes, hours, date, month, day, year, and century). To avoid changing the current time by an incomplete write operation, the current time value is buffered from being written directly to the clock counters. The new data sent replaces the current contents of this input buffer. This time update data is loaded into the clock counters at the rising edge of $\overline{CS}$, which indicates the end of the SPI bus write operation. Collision-detection circuitry ensures that this does not happen coincident with a seconds-counter update to guarantee that accurate time data is being written. This avoids time data changes during a write operation. An incomplete write operation aborts the time-update procedures and the contents of the input buffer are discarded. The clock counter is reset immediately after a write to the seconds register or a burst write to the timekeeping registers. This process ensures that 1s clock tick is synchronous to timekeeping writes.

If single-write operations (Figure 3) are used to write to each of the timekeeping registers, then error checking is needed. If the seconds register is the one to be updated, update it first and then read it back and store its value as the initial seconds. Update the remaining timekeeping registers and then read the seconds register again (final seconds). If initial seconds was 59, ensure it is still 59. If initial seconds was not 59, ensure that final seconds is within 1s of initial seconds. If the seconds register is not to be written to, then read the seconds register first and save it as initial seconds. Write to the required timekeeping registers and then read the seconds register again (final seconds). If initial seconds was 59, ensure it is still 59. If initial seconds was not 59, ensure that final seconds is within 1s of initial seconds.

Although both single writes and burst writes are possible, the most accurate way to write to the timekeeping counters is to do a burst write (Figure 4). In the burst write, the main timekeeping registers (seconds, minutes, hours, date, month, day, year) and the control register are written sequentially. They must be all written to as a group of eight registers, with 8 bytes each, for proper execution of the burst-write function. All seven timekeeping registers and the control register are simultaneously loaded into the clock counters at the rising edge of $\overline{CS}$, at the end of the SPI bus write operation. The worst-case error that can occur between the actual time and the write time update is 1s.

To avoid rollover issues when writing time data to the MAX6916, the remaining time and date registers must be written within 1s of updating the seconds register when using single writes. For burst writes, all eight registers must be written within this period (1s).

The weekday data in the day register increments at midnight. Values that correspond to the day of week are user defined, but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). If invalid values are written to the timekeeping registers, operation becomes undefined.

Registers

Tables 1 and 2 show the register map, as well as the register descriptions for the MAX6916.

Control Register

The control register contains bits for configuring the MAX6916 for custom applications. Bit D0 (BATT ON BLINK) and D1 (BATT LO BLINK) are used to enable a 1Hz blink rate on $\overline{BATT\_ON}$ and $\overline{BATT\_LO}$ when they are active; see the *Battery Test* section for details. D2 (WD TIME) and D3 (WD EN) are used to enable the watchdog function and select its timeout. For details, see the *Watchdog Input* section. D5 (INT/EXT TEST) sets whether the internal resistor ratio or an external resistor ratio is to be used to check for the low-battery condition; see the *Battery Test* section for details. D6 (XTAL EN) enables the crystal-fail-detect circuitry when set. See the *Crystal-Fail Detect* section for details. D7 (WP) is the write-protect bit. Before any write operation to the registers (except the control register) or RAM, bit 7 must be zero. When set to one, the write-protect bit prevents write operations to any register (except the control register) or RAM locations.

Timekeeping and Alarm Thresholds Registers

Time and date data is stored in the timekeeping and alarm threshold registers in BCD format as shown in Table 1. The weekday data in the day register is user defined (a common format is 1 = Sunday, 2 = Monday, etc.).

AM-PM/12–24 Mode

For both timekeeping and alarm threshold registers (Table 1), D7 of the hours register is defined as the 12hr or 24hr mode-select bit. When set to one, the 12hr mode is selected. In the 12hr mode, D5 is the $\overline{AM}$/PM bit with logic one being PM. In the 24hr mode, D5 is the second 10hr bit (20hr to 23hr).

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Table 1. Register Map

FUNCTION	REGISTER ADDRESS A7	A6	A5	A4	A3	A2	A1	A0
CLOCK BURST	R/$\overline{W}$	0	0	0	0	0	0	0
SEC	R/$\overline{W}$	0	0	0	0	0	0	1
MIN	R/$\overline{W}$	0	0	0	0	0	1	0
HR	R/$\overline{W}$	0	0	0	0	0	1	1
DATE	R/$\overline{W}$	0	0	0	0	1	0	0
MONTH	R/$\overline{W}$	0	0	0	0	1	0	1
DAY	R/$\overline{W}$	0	0	0	0	1	1	0
YEAR	R/$\overline{W}$	0	0	0	0	1	1	1
CONTROL	R/$\overline{W}$	0	0	0	1	0	0	0
CENTURY	R/$\overline{W}$	0	0	0	1	0	0	1
ALARM CONFIGURATION	R/$\overline{W}$	0	0	0	1	0	1	0
STATUS	R/$\overline{W}$	0	0	0	1	1	0	0

VALUE	REGISTER FUNCTION D7	D6	D5	D4	D3	D2	D1	D0
0–59	0	10 SEC			1 SEC			
POR STATE	0	0	0	0	0	0	0	0
0–59	0	10 MIN			1 MIN			
POR STATE	0	0	0	0	0	0	0	0
00–23	12/$\overline{24}$	0	10 HR	10 HR	1 HR			
01–12			$\overline{AM}$/PM					
POR STATE	0	0	0	0	0	0	0	0
01–28/29 01–30/31	0	0	10 DATE		1 DATE			
POR STATE	0	0	0	0	0	0	0	1
01–12	0	0	0	10 M	1 MONTH			
POR STATE	0	0	0	0	0	0	0	1
01–07	0	0	0	0	0	WEEKDAY		
POR STATE	0	0	0	0	0	0	0	1
00–99	10 YEAR				1 YEAR			
POR STATE	0	1	1	1	0	0	0	0
	WP	XTAL EN	INT/$\overline{EXT}$ TEST	0	WD EN	WD TIME	BATT LO BLINK	BATT ON BLINK
POR STATE	0	1	0	0	1	0	0	0
00–99	1000 YEAR				100 YEAR			
POR STATE	0	0	0	1	1	0	0	1
	ONE SEC	YEAR	DAY	MONTH	DATE	HR	MIN	SEC
POR STATE	0	0	0	0	0	0	0	0
	XTAL FAIL	DATA VALID	BATT LO	ALM OUT	0	0	0	0
POR STATE	0	0	0	0	0	0	0	0

POR STATE DEFINES THE POWER-ON RESET STATE OF THE REGISTER

Table 1. Register Map (continued)

FUNCTION	REGISTER ADDRESS A7	A6	A5	A4	A3	A2	A1	A0	VALUE	REGISTER FUNCTION D7	D6	D5	D4	D3	D2	D1	D0
BATT TEST	0	0	0	0	1	1	0	1									
ALARM THRESHOLDS:																	
SEC	R/$\overline{W}$	0	0	0	1	1	1	0	0–59	0	10 SEC			1 SEC			
									POR STATE	0	1	1	1	1	1	1	1
MIN	R/$\overline{W}$	0	0	0	1	1	1	1	0–59	0	10 MIN			1 MIN			
									POR STATE	0	1	1	1	1	1	1	1
HR	R/$\overline{W}$	0	0	1	0	0	0	0	00–23	12/$\overline{24}$	0	10 HR / $\overline{\text{AM/PM}}$	10 HR	1 HR			
									01–12								
									POR STATE	1	0	1	1	1	1	1	1
DATE	R/$\overline{W}$	0	0	1	0	0	0	1	01–28/29 01–30/31	0	0	10 DATE		1 DATE			
									POR STATE	0	0	1	1	1	1	1	1
MONTH	R/$\overline{W}$	0	0	1	0	0	1	0	01–12	0	0	0	10 M	1 MONTH			
									POR STATE	0	0	0	1	1	1	1	1
DAY	R/$\overline{W}$	0	0	1	0	0	1	1	01–07	0	0	0	0	0	WEEKDAY		
									POR STATE	0	0	0	0	0	1	1	1
YEAR	R/$\overline{W}$	0	0	1	0	1	0	0	00–99	10 YEAR				1 YEAR			
									POR STATE	1	1	1	1	1	1	1	1
TEST CONFIGURATION (FACTORY RESERVED)	R/$\overline{W}$	0	0	1	0	1	0	1	POR STATE	0	0	0	0	0	0	0	0
RAM REGISTERS:																	
RAM 0	R/$\overline{W}$	0	0	1	1	1	1	1	RAM DATA 0 00h–FFh	X	X	X	X	X	X	X	X
⋮									⋮								
RAM 95	R/$\overline{W}$	1	1	1	1	1	1	0	RAM DATA 95 00h–FFh	X	X	X	X	X	X	X	X
RAM BURST	R/$\overline{W}$	1	1	1	1	1	1	1									

POR STATE DEFINES THE POWER-ON RESET STATE OF THE REGISTER

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Clock-Burst Mode

Addressing the clock-burst register specifies burst-mode operation. In this mode, the first eight clock/calendar registers (seven timekeeping and the control register) can be consecutively read or written to by using the address/command byte 00h for a write or 80h for a read (Table 1). If the write-protect bit is set to one when a write-clock/calendar-burst mode is specified, no data transfer occurs to any of the seven timekeeping registers or the control register. When writing to the clock/calendar registers in the burst mode, the first eight registers must be written to for the data to be transferred; see Table 2.

RAM

The static RAM consists of 96 x 8 bits addressed consecutively in the RAM address/command space. Address/commands (1Fh to 7Eh) are used for RAM writes and address/commands (9Fh to FEh) are used for RAM reads (Table 2).

RAM-Burst Mode

Sending the RAM burst address/command (7Fh for write, FFh for read) specifies burst-mode operation. In this mode, the 96 RAM locations can be consecutively read or written to starting with bit 7 of address/command 1Fh for writes, and 9Fh for reads. A burst read outputs all 96 bytes of RAM. When writing to RAM in burst mode, it is not necessary to write all 96 bytes for the data to transfer; each complete byte written is transferred to the RAM. When reading from RAM, data is output until all 96 bytes have been read, or until the $\overline{CS}$ is driven high.

Status Register

The status register contains individual bits for monitoring the status of several functions of the MAX6916. Bits D0–D3 are unused and always read zero (Table 1). D4 (ALM OUT) reflects the state of the alarm function; see the *Alarm Function* section for details. D5 (BATT LO) indicates the state of the battery connected to V_{BATT}; see the *Battery Test* section for more information. D6 (DATA VALID) alerts the user if all power was lost. See the *Data Valid Bit* section for details. D7 (XTAL FAIL) is the output of the crystal-fail detect circuit. See the *Crystal-Fail Detect* section for details.

Power Control

V_{BATT} provides power as a battery backup. V_{CC} provides the primary power in dual-supply systems where V_{BATT} is connected as a backup source to maintain timekeeping in the absence of primary power. When V_{CC} rises above the reset threshold, V_{RST}, V_{CC} powers the MAX6916. When V_{CC} falls below the reset threshold, V_{RST}, and is less than V_{TRD}, V_{BATT} powers the MAX6916. If V_{CC} falls below the reset threshold, V_{RST}, and is more than V_{TRU}, V_{CC} still powers the MAX6916. The V_{CC} slew rate in power-down is limited to 10V/ms (max) for proper data retention.

V_{OUT} Function

V_{OUT} is an output supply voltage for battery-backed-up devices such as SRAM. When V_{CC} rises above the reset threshold or is greater than V_{BATT}, V_{OUT} connects to V_{CC} (Figure 16). When V_{CC} falls below V_{RST} and V_{BATT}, V_{OUT} connects to V_{BATT}. There is a typical ±100mV hysteresis associated with the switching between V_{CC} and V_{BATT} on the V_{OUT} output. Connect a 0.1µF capacitor from V_{OUT} to GND.

Power-On Reset (POR)

The MAX6916 contains an integral POR circuit that ensures all registers are reset to a known state on power-up. Once either V_{CC} or V_{BATT} rises above 1.6V (typ), the POR circuit releases the registers for normal operation. When V_{CC} or V_{BATT} drops to less than 0.9V (typ), the MAX6916 resets all register contents to the POR defaults.

Oscillator Start Time

The MAX6916 oscillator typically takes 1s to 2s to begin oscillating. To ensure the oscillator is operating correctly, the system software should validate proper timekeeping. This validation is accomplished by reading the seconds register. Any reading with more than 0s, from the POR value of 0s, is a validation of proper startup.

Alarm-Generation Function

The alarm function is configured using the alarm-configuration register and the alarm-threshold registers (Tables 1 and 2). Writing a one to D7 (ONE SEC) in the alarm-configuration register sets the alarm function to occur once every second, regardless of any other setting in the alarm-configuration register or in any of the alarm-threshold registers. When the alarm is triggered, D4 (ALM OUT) in the status register is set to one and the open-drain alarm output $\overline{ALM}$ goes low. The alarm is cleared by reading or writing to the alarm-configuration register or by reading or writing to any of the alarm-threshold registers. This process resets the $\overline{ALM}$ output to a high and the ALM OUT bit to zero.

When D7 (ONE SEC) is set to zero in the alarm-configuration register, then the alarm function is set by the remaining bits in the alarm-configuration register and the contents of the respective alarm-threshold register. For example, writing 01h (0000 0001) to the alarm-configuration register causes the alarm to trigger every time the seconds-timekeeping register matches the seconds alarm-threshold register (i.e., once every minute on a specific second). Writing 02h (0000 0010) to the alarm-configuration register causes the alarm to

Table 2. Hex Register Address and Description

WRITE ADDRESS/COMMAND (HEX)	READ ADDRESS/COMMAND (HEX)	DESCRIPTION	POR SETTING (HEX)
00	80	Clock burst	N/A
01	81	Seconds	00
02	82	Minutes	00
03	83	Hour	00
04	84	Date	01
05	85	Month	01
06	86	Day	01
07	87	Year	70
08	88	Control	48
09	89	Century	19
0A	8A	Alarm configuration	00
0C	8C	Status	00
0D	N/A	Battery test	N/A
0E	8E	Seconds alarm threshold	7F
0F	8F	Minutes alarm threshold	7F
10	90	Hours alarm threshold	BF
11	91	Date alarm threshold	3F
12	92	Month alarm threshold	1F
13	93	Day alarm threshold	07
14	94	Year alarm threshold	FF
15	95	Test configuration	00
1F	9F	RAM 0	Indeterminate
20	A0	RAM 1	Indeterminate
21	A1	RAM 2	Indeterminate
22	A2	RAM 3	Indeterminate
23	A3	RAM 4	Indeterminate
•	•	•	•
•	•	•	•
•	•	•	•
7A	FA	RAM 91	Indeterminate
7B	FB	RAM 92	Indeterminate
7C	FC	RAM 93	Indeterminate
7D	FD	RAM 94	Indeterminate
7E	FE	RAM 95	Indeterminate
7F	FF	RAM BURST	N/A

trigger on a minutes match (i.e., once every hour). Writing a 4Fh (0100 1111) to the alarm configuration register causes the alarm to be triggered on a specific second, of a specific minute, of a specific hour, of a specific date, of a specific year.

When setting the alarm-threshold registers, ensure that

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both the hour-timekeeping register and the hour-alarm-threshold register are using the same hour format (either 12hr or 24hr format).

The alarm function as well as the $\overline{ALM}$ output are operational in both V_{CC} and battery-backup mode.

Crystal-Fail Detect

The crystal-fail detect circuit looks for a loss of oscillation from the 32.768kHz oscillator for 30 cycles (typ) or more. Both the control register and the status register are used in the crystal-failure detection scheme (Table 1).

The crystal-fail detect circuit sets the XTAL FAIL bit in the status register to one for a crystal failure and to zero for normal operation. Once the status register is read, the XTAL FAIL bit is reset to zero, if it was previously one. If the crystal-fail-detect circuit continues to sense a failed crystal, then the XTAL FAIL bit is set again.

On initial power-up, the crystal-fail detect circuit is enabled. Since it takes a while for the low-power, 32.768kHz oscillator to start, the XTAL FAIL bit in the status register can be set to one, indicating a crystal failure. The XTAL FAIL bit should be polled a number of times to see if it is set to zero for successive polls. If the polling is far enough apart, a few polled results could guarantee that a maximum of 10s had elapsed since power-on, at which time the oscillator would be considered truly failed if the XTAL FAIL bit remains one.

On subsequent power-ups, when XTAL EN is set to one, if XTAL FAIL is set to one, time data should be considered suspect.

The crystal-fail-detection circuit functions in both V_{CC} and V_{BATT} modes when the XTAL EN bit is set in the control register.

Manual Reset Input

A logic-low on $\overline{MR}$ asserts $\overline{RESET}$. $\overline{RESET}$ remains asserted while $\overline{MR}$ is low, and for t_{RP} after it returns high (Figure 7). $\overline{MR}$ has an internal pullup resistor, so it can be left open if it is not used. Internal debounce circuitry requires a minimum low time on the $\overline{MR}$ input of 1µs with 35ns maximum glitch immunity.

Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state. The MAX6916's µP supervisory circuit asserts a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. The $\overline{RESET}$ output is guaranteed to be active for $0V < V_{CC} < V_{RST}$, provided V_{BATT} is greater than V_{BATT} (min). If V_{CC} drops below and then exceeds the reset threshold, an internal timer keeps $\overline{RESET}$ active for the reset timeout period t_{RP}; after this interval, $\overline{RESET}$ becomes

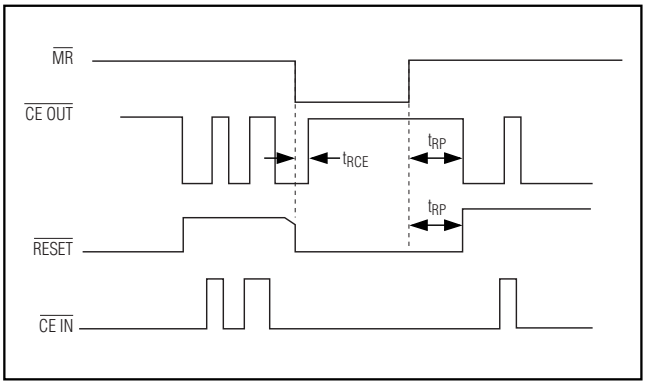

Figure 7. Manual Reset Timing Diagram

inactive high. This condition occurs at either power-up or after a V_{CC} brownout.

The $\overline{RESET}$ output is also activated when the watchdog interrupt function is enabled but no transition is detected on the WDI input. In this case, $\overline{RESET}$ is active for the period t_{RP} before becoming inactive again. When $\overline{RESET}$ is active, all inputs—WDI, $\overline{MR}$, $\overline{CE\_IN}$, DIN, $\overline{CS}$, and SCLK—are disabled. DOUT is also disabled.

The MAX6916EO30 is optimized to monitor 3.0V ±10% power supplies. Except when $\overline{MR}$ is asserted, $\overline{RESET}$ is not active until V_{CC} falls below 2.7V (3.0V - 10%), but is guaranteed to occur before the power supply falls below 2.5V (3.0V - 15%).

The MAX6916EO33 is optimized to monitor 3.3V ±10% power supplies. Except when $\overline{MR}$ is asserted, $\overline{RESET}$ is not active until V_{CC} falls below 3.0V (3.0V is just above 3.3V - 10%), but is guaranteed to occur before the power supply falls below 2.8V (3.3V - 15%).

The MAX6916EO50 is optimized to monitor 5.0V ±10% power supplies. Except when $\overline{MR}$ is asserted, $\overline{RESET}$ is not active until V_{CC} falls below 4.5V (5.0V - 10%), but is guaranteed to occur before the power supply falls below 4.2V (4.2V is just below 5.0V - 15%).

Negative-Going V_{CC} Transients

The MAX6916 is relatively immune to short-duration negative transients (glitches) while issuing resets to the µP during power-up, power-down, and brownout conditions. Therefore, resetting the µP when V_{CC} experiences only small glitches is usually not recommended. Typically, a V_{CC} transient that goes 150mV below the reset threshold and lasts for 50µs or less does not cause a reset pulse to be issued. A 0.1µF capacitor mounted close to the V_{CC} pin provides additional transient immunity.

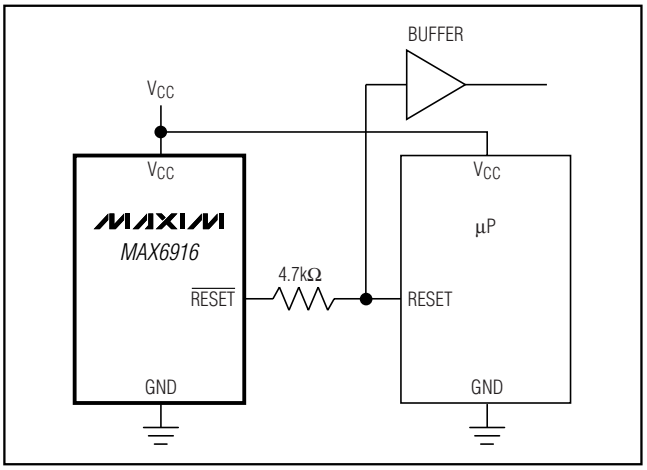

Figure 8. Interfacing to µP with Bidirectional Reset I/O

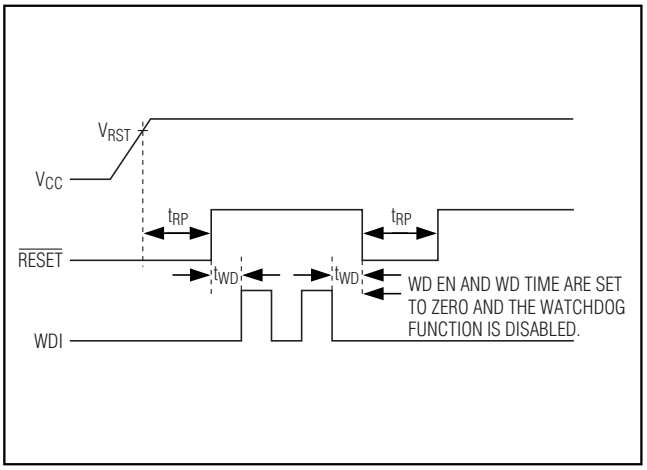

Figure 9. Watchdog Timing Diagram

Interfacing to Microprocessors with Bidirectional Reset Pins

Microprocessors with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the MAX6916 $\overline{RESET}$ output. If, for example, the $\overline{RESET}$ output is driven high and the µP wants to pull it low, indeterminate logic levels can result. To correct this, connect a 4.7kΩ resistor between the $\overline{RESET}$ output and the µP reset I/O as shown in Figure 8. Buffer the $\overline{RESET}$ output to other system components.

Battery-On Output

The battery-on output, $\overline{BATT\_ON}$, is an open-drain output that indicates when the MAX6916 is powered from the backup-battery input, V_{BATT}. When V_{CC} falls below the reset threshold, V_{RST}, and below V_{BATT}, V_{OUT} switches from V_{CC} to V_{BATT} and $\overline{BATT\_ON}$ becomes low. When V_{CC} rises above the reset threshold, V_{RST}, V_{OUT} reconnects to V_{CC} and $\overline{BATT\_ON}$ becomes high (open-drain output with pullup resistor). If desired, the $\overline{BATT\_ON}$ output can be register selected, through the BATT ON BLINK bit in the control register, to toggle on and off (0.5s on, 0.5s off) when active. The POR default is logic zero for no blink.

Watchdog Input

The watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within the register-selectable watchdog-timeout period, $\overline{RESET}$ is asserted for t_{RP}. At the same time, the WD EN and WD TIME bits in the control register (Table 1) are reset to zero and can only be set again by writing the appropriate command to the control register. Thus, once a $\overline{RESET}$ is asserted due to a watchdog timeout, the watchdog function is disabled (Figure 9).

WDI can detect pulses as short as t_{WDI}. Data bit D2 in the control register controls the selection of the watchdog-timeout period. The power-up default is 1.6s (D2 = 0). A reset condition returns the timeout to 1.6s (D2 = 0). If D2 is set to one, then the watchdog-timeout period is changed to 200ms. Data bit D3 in the control register is the watchdog-enable function. A logic zero disables the watchdog function, while a logic one enables it. The POR state of WD EN is logic one, or the watchdog function is enabled. Disable the watchdog function by writing a zero to the WD EN bit in the control register, within the 1.6s POR default timeout after power-up.

WDI does not include a pulldown or pullup feature. For this reason, WDI should not be left floating. When the WD EN bit in the control register is set to zero, WDI should be connected to V_{CC} or GND. WDI is disabled and does not draw cross-conduction current when V_{CC} falls below V_{RST}.

Watchdog Software Considerations

There is a way to help the watchdog-timer monitor software execution more closely, which involves setting and resetting the watchdog input at different points in the program rather than "pulsing" the watchdog input. This technique avoids a "stuck" loop, in which the watchdog timer would continue to be reset within the loop, keeping the watchdog from timing out. Figure 10 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should "hang" in any subroutine, the problem would quickly be corrected since the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset to be issued.

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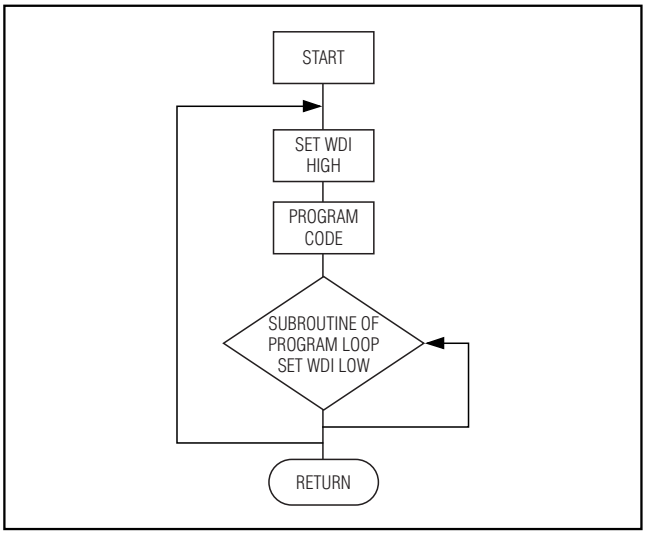

Figure 10. Watchdog Flow Diagram

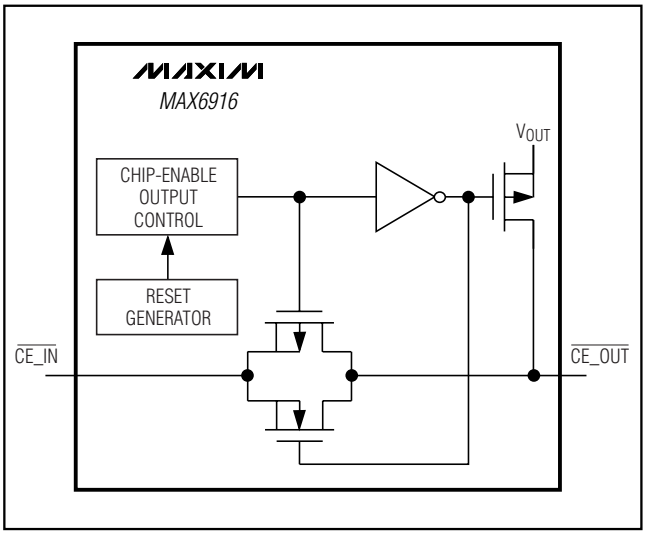

Figure 11. Chip-Enable Gating

Chip-Enable Gating

Internal gating of chip-enable (CE) signals prevents erroneous data from corrupting external SRAM in the event of an undervoltage condition. The MAX6916 uses a transmission gate from $\overline{CE\_IN}$ to $\overline{CE\_OUT}$ (Figure 11). During normal operation ($\overline{RESET}$ inactive), the transmission gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the external SRAM. The short CE propagation delay from $\overline{CE\_IN}$ to $\overline{CE\_OUT}$ enables the MAX6916 to be used with most microprocessors. If $\overline{CE\_IN}$ is low when reset asserts, $\overline{CE\_OUT}$ remains low for t_{RCE} to permit completion of the current write cycle.

Chip-Enable Input

The CE transmission gate is disabled and $\overline{CE\_IN}$ is high impedance (disabled mode) while $\overline{RESET}$ is active. During a power-down sequence when V_{CC} passes the reset threshold, the CE transmission gate disables and $\overline{CE\_IN}$ immediately becomes high impedance if the voltage at $\overline{CE\_IN}$ is high. If $\overline{CE\_IN}$ is low when $\overline{RESET}$ becomes active, the CE transmission gate disables at the moment $\overline{CE\_IN}$ goes high or t_{RCE} after $\overline{RESET}$ is active, whichever occurs first (see the *Chip-Enable Timing* section). This condition permits the current write cycle to complete during power-down. The CE transmission gate remains disabled and $\overline{CE\_IN}$ remains high impedance (regardless of $\overline{CE\_IN}$ activity) for most of the reset-timeout period (t_{RST}) any time a $\overline{RESET}$ is generated. When the CE transmission gate is enabled, the impedance of $\overline{CE\_IN}$ appears as a 46Ω (typ) load in series with the load at $\overline{CE\_OUT}$.

The propagation delay through the CE transmission gate depends on V_{CC}, the source impedance of the driver connected to $\overline{CE\_IN}$, and the loading on $\overline{CE\_OUT}$ (see the Chip-Enable Propagation Delay vs. $\overline{CE\_OUT}$ Load Capacitance graph in the *Typical Operating Characteristics*). For minimum propagation delay, the capacitive load at $\overline{CE\_OUT}$ should be minimized, and a low-output-impedance driver should be used on $\overline{CE\_IN}$ (Figure 12).

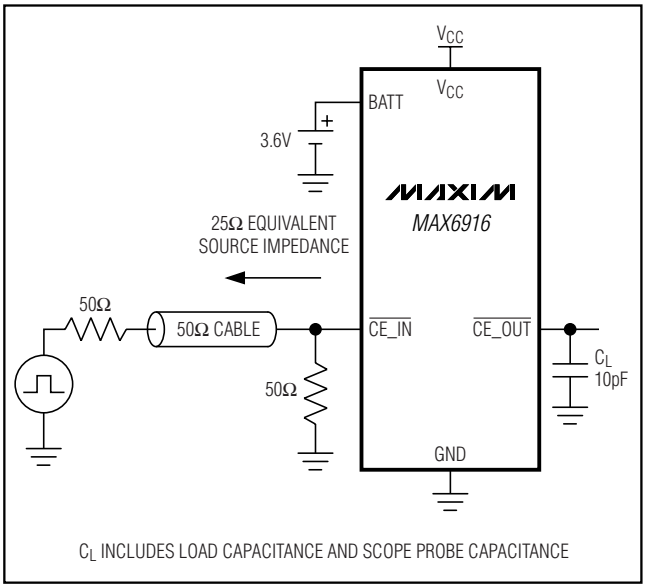

Figure 12. Propagation Delay Test Circuit

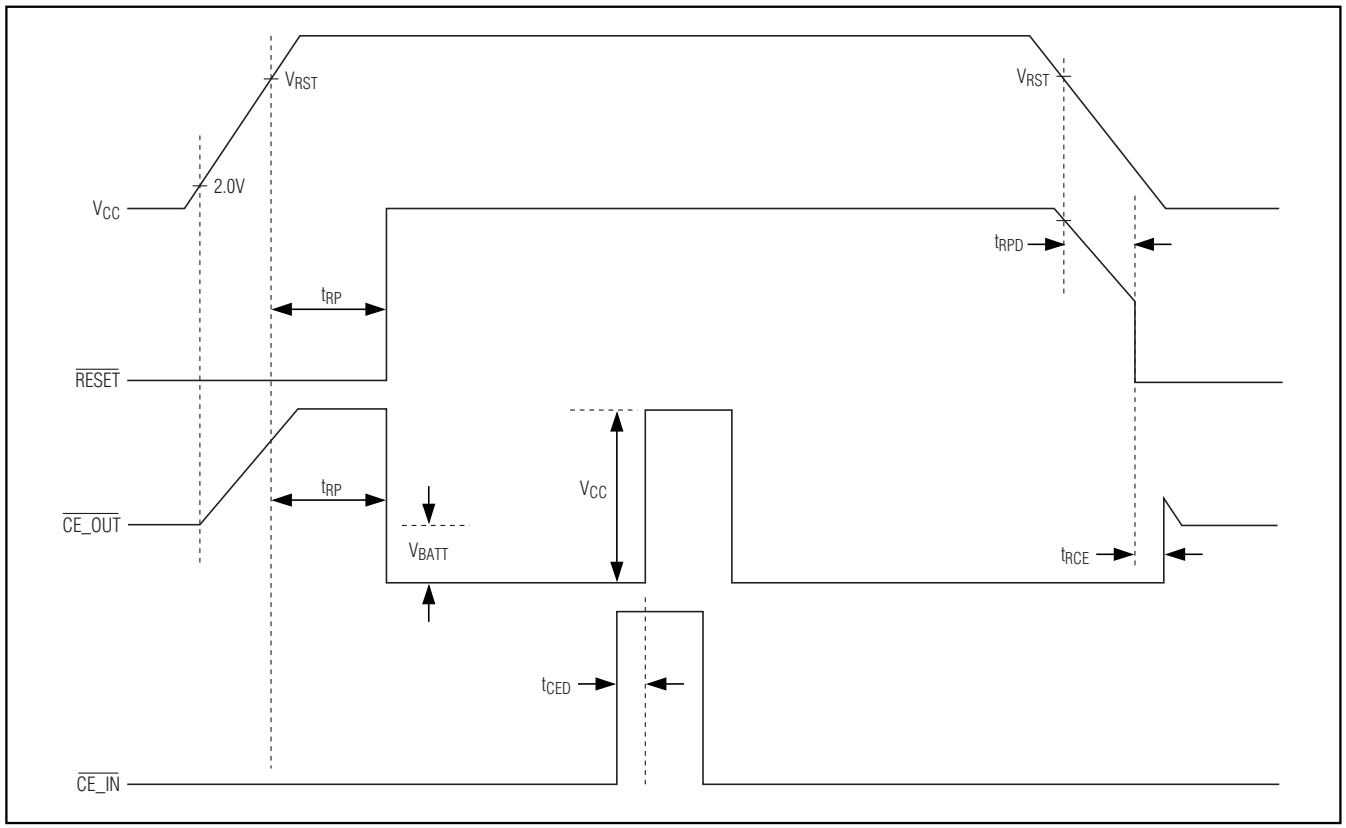

Figure 13. Chip-Enable Timing Diagram

Chip-Enable Output

When the CE transmission gate is enabled, the impedance seen at $\overline{CE\_OUT}$ is equivalent to a 46Ω (typ) resistor in series with the source driving $\overline{CE\_IN}$. In the disabled mode, the transmission gate is off and an active pullup connects $\overline{CE\_OUT}$ to V_{OUT} (see Figures 11 and 13). This pullup turns off when the transmission gate is enabled.

Test Configuration Register

This is a read-only register.

Data Valid Bit

DATA VALID has a POR setting of zero, indicating that the data in the MAX6916 RTC is not guaranteed to be valid (Table 1). A read of the status register sets the DATA VALID bit to one, indicating valid data in the MAX6916 RTC. In a system that uses a backup power supply, the DATA VALID bit should be set to one by the system software on first system power-up by reading the status register. After that, any time the system recovers from a reset condition caused by $V_{CC} < V_{RST}$, the DATA VALID bit can be read to see if the data stored during operation from the backup power supply is still valid (i.e., the backup power supply did not drop out). A one indicates valid data, and a zero indicates corrupted data. Any time the internal supply to the MAX6916 (either V_{BATT} or V_{CC} depending upon the operating conditions) drops below 1.5V to 1.6V (typ), the DATA VALID bit is set to zero even if it has recently been set by a read of the status register.

Battery Test

Battery-Test Normal Operation

In normal operation, the battery-test circuitry uses the control register POR settings of INT/EXT TEST, which is set to logic-low as default (Table 1). In this mode, all battery-test load resistors and threshold settings are internal. When V_{CC} rises above V_{RST}, the MAX6916 automatically performs one power-on battery monitor test. Additionally, a battery check is performed every time that a reset is issued, either from a manual reset or from a watchdog timeout. After that, periodic battery voltage monitoring at the factory-programmed time interval of 24hr begins while V_{CC} is applied.

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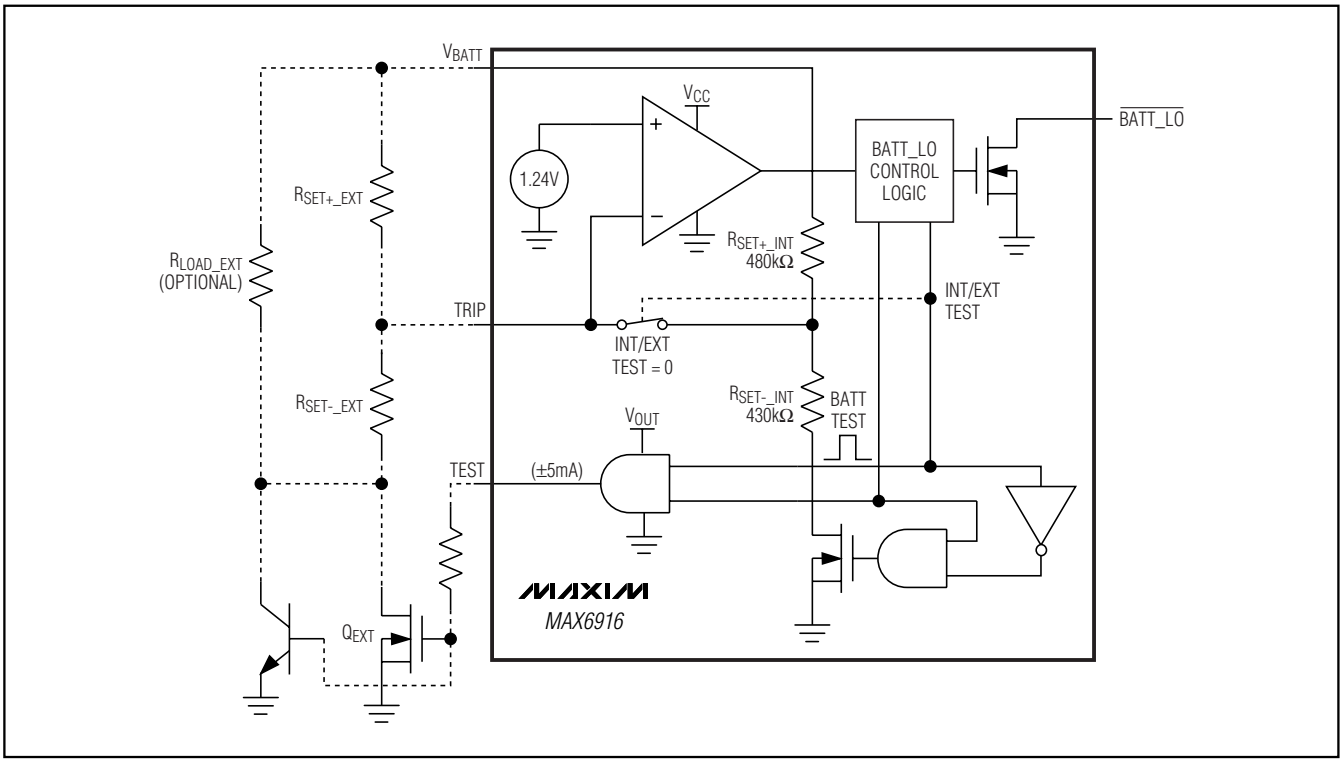

Figure 14. MAX6916 Battery Load and Test Circuit

After each 24hr period (t_{BTCN}) has elapsed, the MAX6916 connects V_{BATT} to an internal 0.91MΩ (typ) test resistor (R_{SET+_INT} + R_{SET-_INT}) for 1s (t_{BTPW}) (Figure 14). During this 1s, if V_{BATT} falls below the factory-programmed battery trip point V_{BTP}, the open-drain, battery-low output, $\overline{BATT\_LO}$, is asserted active low and the BATT LO bit in the status register is set to one. The $\overline{BATT\ LO}$ output can be register selected to toggle at a 1Hz rate (0.5s on, 0.5s off) when active. Once $\overline{BATT\ LO}$ is active, the 24hr tests stop until a fresh battery is inserted and $\overline{BATT\ LO}$ is cleared by writing any data to the battery test register at address 0x0D (Figure 15). Writing to this register performs a battery test and provided that the fresh battery is not low, deactivates the $\overline{BATT\ LO}$ output and resets BATT LO in the status register. Normal 24hr testing resumes. If a different load or $\overline{BATT\ LO}$ thresholds are desired for testing the backup battery, then external program resistors can be used in conjunction with the TRIP and TEST inputs (see the *Battery-Test Control Register and Other Test Options* section).

Battery replacement following $\overline{BATT\_LO}$ activation should be done with V_{CC} nominal and not in battery-backup mode so that SRAM data is not lost. Alternatively, if SRAM data need not be saved, the battery can be replaced with the V_{CC} supply removed. If a battery is replaced in battery-backup mode, sufficient time must be allowed for the voltage on the V_{OUT} output to decay to zero. This timing ensures that the freshness-seal mode of operation has been reset and is active when V_{CC} is powered up again. If insufficient time is allowed, then V_{CC} must exceed V_{BATT} during the subsequent power-up to ensure that the MAX6916 has left battery-backup mode (Figure 16).

The MAX6916 does not constantly monitor an attached battery because such monitoring would drastically reduce the life of the battery. As a result, the MAX6916 only tests the battery for 1s every 24hr. If a good battery (one that has not been previously flagged with $\overline{BATT\_LO}$) is removed between battery tests, the MAX6916 does not immediately sense the removal and does not activate $\overline{BATT\_LO}$ until the next-scheduled battery test. For this reason, a software-commanded battery test should be performed after a battery replacement by writing any data to the battery-test register at address 0Dh.

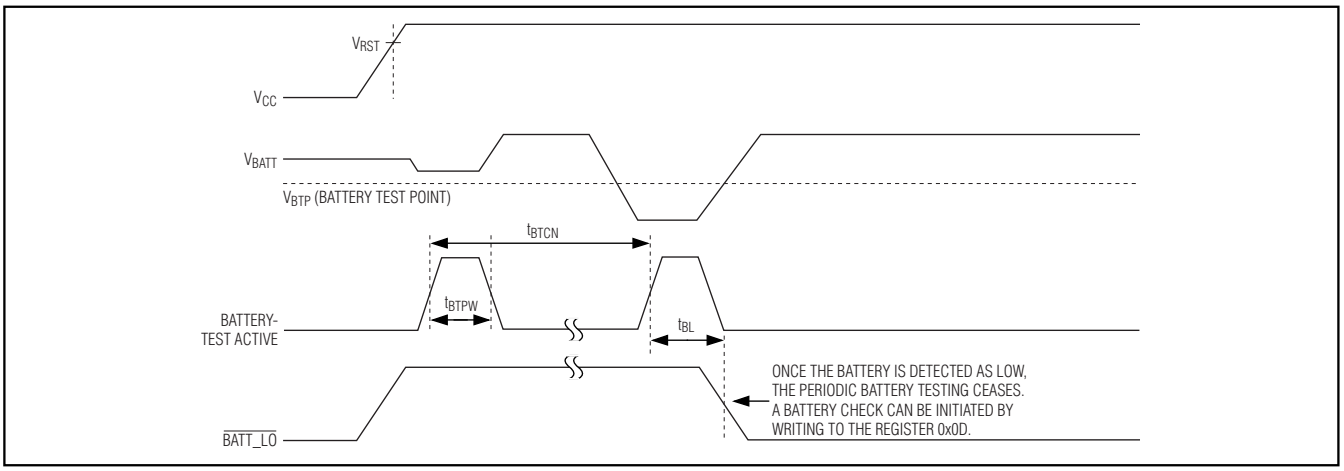

Figure 15. Battery Test Timing Diagram

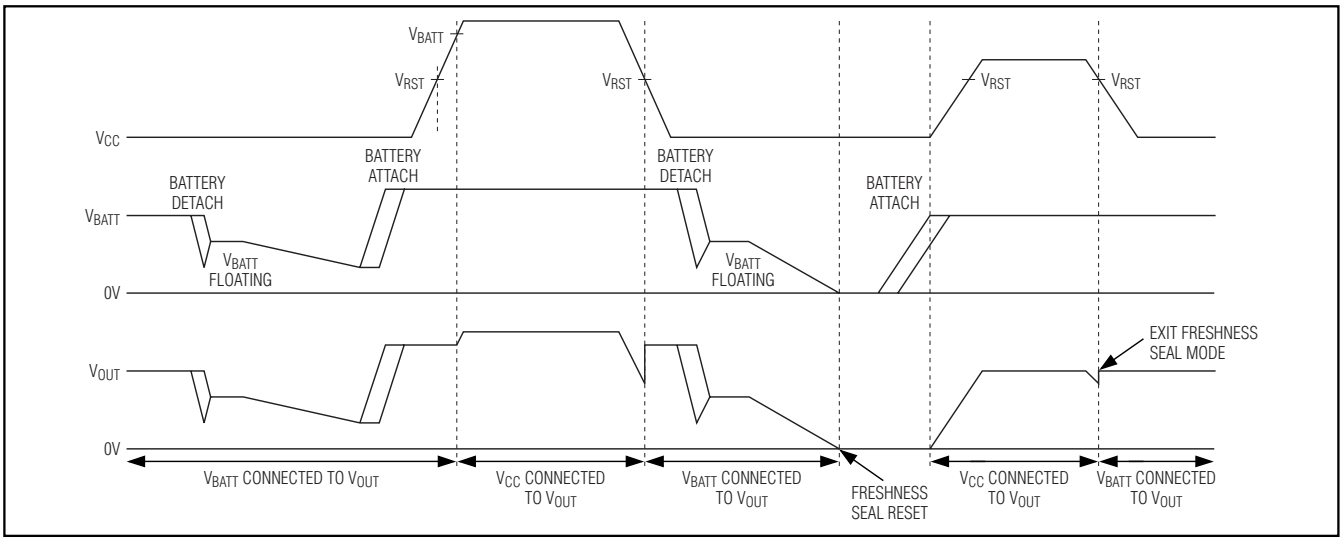

Figure 16. Battery Switchover Diagram

Battery monitoring is only a useful technique when testing can be done regularly over the entire life of a lithium battery. Because the MAX6916 only performs battery monitoring when V_{CC} is nominal, systems that are powered down for excessively long periods can completely drain their lithium cells without receiving any advanced warning. To prevent such an occurrence, systems using the MAX6916 battery-monitoring feature should be powered up periodically (at least every few months) in order to perform battery testing. Furthermore, anytime $\overline{BATT\_LO}$ is activated on the first battery test after a power-up, data integrity should be checked through a checksum or other technique. Timekeeping data would also be suspect and should be checked for accuracy against an accurate known reference.

Freshness-Seal Mode

When the battery is first attached to the MAX6916 without V_{CC} power applied, the device does not immediately provide battery-backup power to V_{OUT} (Figure 16). Only after V_{CC} exceeds V_{RST} and later falls below both V_{RST} and V_{BATT} does the MAX6916 leave freshness-seal mode and provide battery-backup power. This mode allows a battery to be attached during manufacturing but not used until after the system has been activated for the first time. As a result, no battery energy is drained during storage and shipping.

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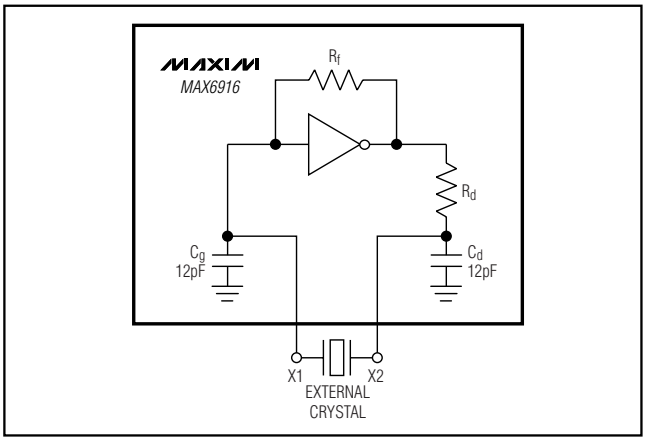


Figure 17. Oscillator Functional Schematic

Battery-Test Control Register and Other Test Options

There are two warning formats for the BATT_LO and BATT_ON outputs. By setting D0 (BATT ON BLINK) and/or D1 (BATT LO BLINK) in the control register to one, the respective warning output toggles on every 0.5s and off every 0.5s when set to active low by the internal MAX6916 logic. This setting allows a more noticeable warning indicator in systems where an LED is connected as a status or warning light for the end user. The POR default settings of zero leave these outputs set to logic-low when they are active.

D5 (INT/EXT TEST) selects whether the battery test circuit is configured as internal or external (Table 1). If D5 is set to zero (default value), then the internal resistor-divider is used between V_{BATT} and GND to select the battery-low trip point (Figure 14). The internal resistors, R_{SET+_INT} and R_{SET-_INT}, are used to divide V_{BATT} in half, as well as to provide the battery-test-load resistance of 0.91MΩ (typ).

If D5 (INT/EXT TEST) is set to one, then the two external resistors, R_{SET+_EXT} and R_{SET-_EXT}, are used to divide V_{BATT} down to the ratio for a trip point set at TRIP of 1.24V (V_{TRIP}) (typ). R_{SET+_EXT} plus R_{SET-_EXT} in series provide the load resistance used during the 1s every-24hr-battery test. If additional load resistance is desired, then an external load resistor, R_{LOAD_EXT}, can be placed between V_{BATT} and the collector or drain of the transistor driven by TEST. The equivalent load resistance used to test the battery is then R_{LOAD_EXT} in parallel with the series combination of R_{SET+_EXT} plus R_{SET-_EXT}. In this mode, the internal resistors are removed from TRIP and are not used as a load during the battery-test pulse. TEST pulses high to perform the battery test and remains low between tests.

One final battery-test feature of the MAX6916 is the software write address/command of 0Dh that forces a 1s battery test to be performed every time it is sent.

Applications Information

Crystal Selection

Connect a 32.768kHz watch crystal directly to the MAX6916 through pins 9 and 10 (X1, X2) (Figure 17). Use a crystal with a specified load capacitance (C_L) of 6pF. Refer to Applications Note 616: *Considerations for Maxim Real-Time Clock Crystal Selection* from the Maxim website (www.maxim-ic.com) for more information regarding crystal parameters and crystal selection, as well as a list of crystal manufacturers.

When designing the PC board, keep the crystal as close to the X1 and X2 pins of the MAX6916 as possible. Keep the trace lengths short and small to reduce capacitive loading and prevent unwanted noise pickup. Place a guard ring around the crystal and connect the ring to ground to help isolate the crystal from unwanted noise pickup. Keep all signals out from beneath the crystal and the X1 and X2 pins to prevent noise coupling. Finally, an additional local ground plane on an adjacent PC board layer can be added under the crystal to shield it from unwanted pickup from traces on other layers of the board. This plane should be isolated from the regular PC board ground, connected to the GND pin of the MAX6916, and needs to be no larger than the perimeter of the guard ring. Ensure that this ground plane does not contribute to significant capacitance between the signal line and ground on the connections that run from X1 and X2 to the crystal. See Figure 18.

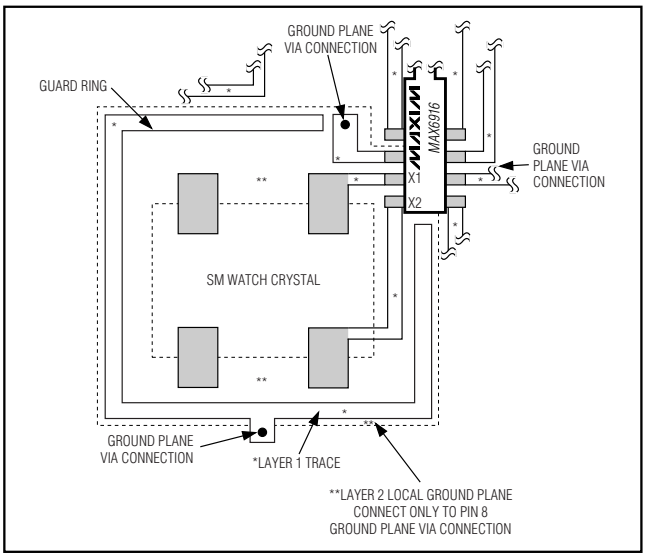


Figure 18. Crystal Layout

SPI-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

For frequency stability over temperature, refer to the Applications Note 617: *Real-Time-Clock Selection and Optimization* from the Maxim website (www.maxim-ic.com.)

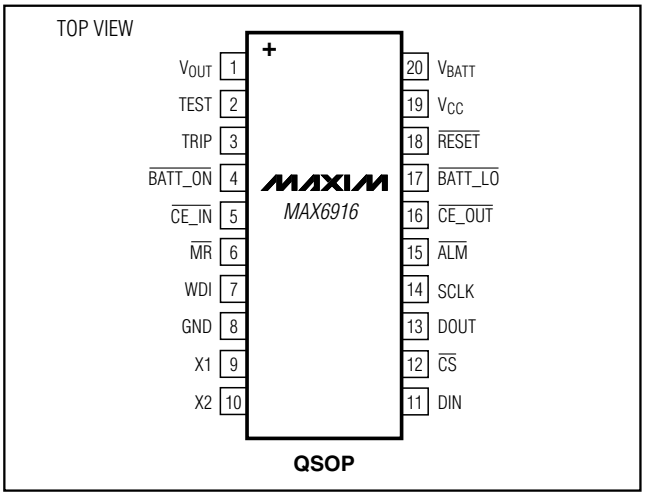
Selector Guide

PART	SUPPLY VOLTAGE (V)
MAX6916EO30	3.0
MAX6916EO33	3.3
MAX6916EO50	5.0

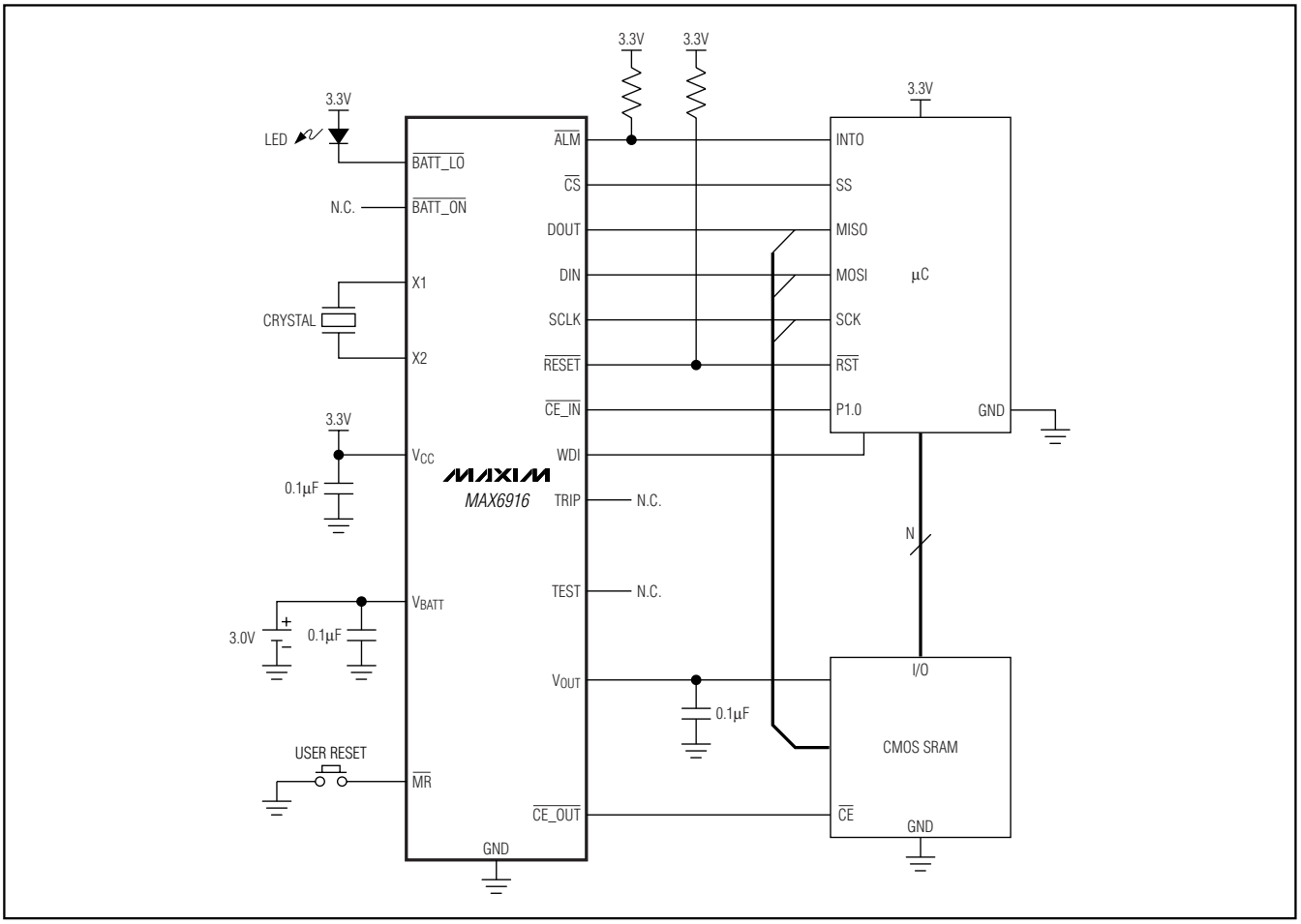
Chip Information

PROCESS: CMOS

Pin Configuration



Typical Application Circuit

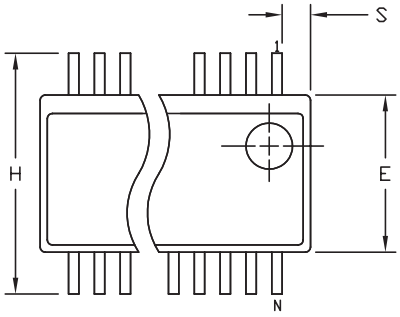


SPI-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

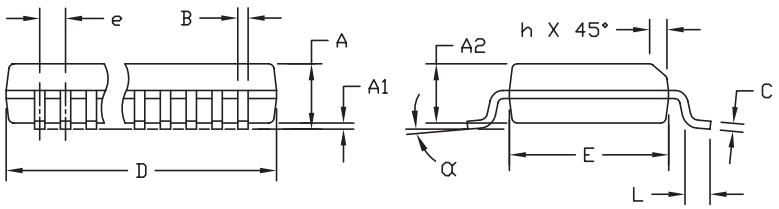
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	E	1/1